UPDATED SCHEME OF EXAMS. & SYLLABI FOR B.SC.ELECTRONICS OF SEM I & SEM II

Paper No.	Title of Paper	Max. Marks		Exam Duration
		External	Internal	
Semester –I				
I	Electronic Devices and Circuits-I (Th)	40	10	3hrs
II	Digital Electronics-I(Th)	40	10	3hrs
Semester-II				
I	Electronic Devices and Circuits –II(Th)	40	10	3hrs
II	Network Analysis(Th)	40	10	3hrs
III	PRACTICAL	100		3hrs

NOTE: 20% INTERNAL ASSESSMENT ON THE BASIS OF CLASS TESTS, ATTENDANCE AND ASSESSMENT .

Instructions for Examiner :

Course: Bachelor of Science (B.Sc.) 1st Year

Subject: Electronics

Examination Scheme for Semester 1 & 2

I. Theory Papers(Semester System of Examination)

1. Syllabus in each Theory Paper is divided in 4 units.

   i. A Student is required to attempt 5 questions in all.

   ii. Question No 1 is compulsory, consisting of short answer type questions based on all the 4 units.

   iii. Two questions will be set from each unit. A student is required to attempt one question from each unit.

   iv. All questions carry equal marks.

2. Use of simple calculator is permissible.

3. Instructions should be imparted using SI system of units. Familiarity with CGS system of units should also be ensured.

4. Distribution of Marks :

   Paper I –40+10*= 50 marks of 3 hours duration.

   Paper II – 40+10*=50 marks of 3 hour duration.

* For each paper question paper will be of 40 marks and 10 marks in each theory paper are awarded through internal assessment in each semester.

II. Practical Paper (Annual Examination System)

i) The Practical examination will be held at the end of 2nd semester in two sittings of three hours each with First sitting starting in the evening session of the first day and second sitting in the following morning session.

ii) A candidate is required to perform minimum of 6 experiment in each section out of the list provided during course of study in Semester I and Semester II and is required to perform one experiment from each section in examination. Experiment from one section in First Sitting and experiment from other section in Second Sitting.

iii) Distribution of Marks :

Paper III – 100 Marks of 3+3 Hours duration

Lab Record: 20

Experiments: 20 + 20

Viva/Voce : 20+20

iv) Maximum 10 students in one group during course of study and also in Examination.

Semester-I

Subject: Electronics

Paper: I (Theory)

Nomenclature:-Electronic Devices and Circuits-I

Max. Marks: 40+10

Time: 3hrs.

Unit -I

Intrinsic and Extrinsic semiconductors, Energy Band diagram, drift and diffusion current in semiconductors(Basic idea only), Junction diode and its characteristics, Space charge capacitor and diffusion capacitor (simple idea only), Zener diode, Voltage Regulation using Zener Diode (Basic Idea), shunt and series clipping ckts., clamping circuit .

Unit-II

Rectifiers: HWR, FWR, Bridge FWR, rectifier parameters.

Filter circuits: L, C, LC (Calculation of ripple factor). Voltage multiplier Ckts

Unit –III

Junction Transistor: Potential curves in unbiased and biased transistor, Transistor current components, Early effect, Static Characteristics of CB & CE configuration, active, cut off and saturation regions.

Transistor as an Amplifier, Transistor current gains (Alpha, Beta, Gama)

Unit-IV

Ebers-moll model of transistor, Hybrid-Model of transistor, Emitter follower, calculation of transistor amplifier parameters using h-model, comparison of transistor amplifier configuration, millers – theorem and its dual

Ref.:

1. Integrated Electronics by Millman and Halkias.
2. Basic Electronics and Linear Circuits by NN Bhargava, DC Kulshreshtha (TTTI)

Semester-I

Subject-Electronics

Paper: II (Theory)

Nomenclature:-Digital Electronics-I

Max. Marks: 40+10

Time: 3hrs.

Unit-I

Number systems: Binary, Octal, Hexadecimal number system and base conversions, Binary Arithmatic operations , 1's and 2's complement representation and there arithmetic. Binary codes-BCD, Grey, cyclic, ASCII, EBCDIC, Parity Bit Code, Unicode, Sequential Code.

Unit-II

Logic Gates: AND,OR, NOT,XOR,XNOR,NOR,NAND (Definition, Symbols& Truth table).

Boolean Algebra: Postulates, Duality Principal , De Morgan's Law, Simplification of Boolean Identities , Standard SOP & POS Forms, Simplification using K-map, don't care condition implementation of SOP & POS form using NAND and NOR Gate.

Unit III

Bipolar Logic families , Unipolar Logic families , characteristics of Digital IC's. Resistance-Transistor Logic (RTC), Direct Coupled Logic(DCTL), Diode Transistor Logic .

Unit-IV

High Treshhold Logic, TTL, Schott-ky TTL, ECL, MOS logic, CMOS Logic

Ref.:

1. Digital Electronics by R.P. Jain

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iii) Distribution of Marks :

Paper III – 100 Marks of 3+3 Hours duration

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Experiments: 20 + 20

Viva/Voce : 20+20

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Semester-II

Subject: Electronics

Paper: I (Theory)

Nomenclature: - Electronic Devices and Circuits –II

Max. Marks: 40+10

Time: 3hrs.

Unit-I

Why Bias a Transistor, Selection of Operating Point, Need for Bias Stabilization, Requirement of a Biasing Circuit, Different Biasing Circuits, Fixed-Bias Circuit, Collector-to-base Bias Circuit.

Unit-II

Bias Circuit with Emitter Resistor, Voltage Divider Biasing Circuit, Emitter-Bias Circuit, Gain of a multi-stage amplifier.

Unit-III

How to couple two stages, Resistance-Capacitance Coupling, Transformer Coupling, Direct Coupling, Frequency Response Curve of an RC-Coupled Amplifier, Fall of Gain in Low-frequency Range, Does gain fall in high Frequencies, Bandwidth of an amplifier.

Unit-IV

Junctions Field Effect Transistor, Qualitative Description of JFET, Drain and transfer characteristics of JFET, FET small signal low frequency model, CS & CD low frequency model,

MOSFET -Depletion and enhancement and their drain & transfer characteristics.

Ref.:

1. Basic Electronics and Linear Circuits by NN Bhargava, D C Kulshreshtha
2. Integrated Electronics by Millman and Halkian

Semester –II
Subject: Electronics
Paper: II (THEORY)

Nomenclature: -Network Analysis

Max. Marks: 40+10

Time: 3hrs.

Unit-I

Kirchhofs Voltage Law, Kirchhofs Current Law, Mesh Analysis, Nodal Analysis, Source

Transformation Technique, Star-Delta Transformation, Superposition Theorem, Thevenin's Theorem.

Unit-II

Norton's Theorem, Reciprocity Theorem, Compensation Theorem, Maximum Power Transfer Theorem, Duals and Duality, Tellegen's Theorem, Millman's Theorem.

Unit –III

Two–port Network ,open Circuit Impedance(Z) Parameters, Short Circuit Admittance (Y) Parameters, Transmission(ABCD) Parameters, Inverse Transmission (A'B'C'D') Parameters, Hybrid(h) Parameters, Inverse Hybrid(g) Parameters , Inter Relationships of different Parameters

Unit –IV

Inter Connection of Two – Port Networks, T and π Representation, Terminated Two-Port Networks, Lattice Networks, Image Parameters.

Ref.:

1. Circuits and Networks by A. Sudhakar, Shyammohan

SEMESTER 1 & 2

SUBJECT: ELECTRONICS

PAPER: III (PRACTICAL)

Max. Marks: 100

Time: 3+3 hrs.

Section-A

1. To study the V-I characteristics of PN junction diode.
2. To study the zener diode as voltage regulator.
3. To study half wave voltage multiplier Ckt. Using diode.
4. To study HWR and FWR and measurement of ripple factor with and with C filter.
5. To study diode as shunt clipping clement.
6. To study diode as clamping element.
7. Study of CB characteristics and calculate H parameter from graph.
8. Study of CE characteristics and calculate H parameter from graph.
9. Study of JFET characteristics.
10. To measure Av. Ai. Ap. In CB. CC Transistor amplifier.
11. Study of fixed bias arrangement for transistor.

Section-B

1. Measurement of voltage. Time period and phase-shift Biasing CRO.
2. Measurement of resistance by colour code method and using M/M and to design a potential divider arrangement and familiarization of components such as capacitors, potentiometer, diode, transistors, etc.
3. Study of basis logic gate (AOI).
4. Study of DTL NAND gate.
5. Study of TTL NANA gate.
6. Digital trainer using AOI.
7. Digital trainer using NAND.
8. To study of RC Ckts. As integrating and differentiating Ckts.
9. To verify maximum power transfer theorem for DC network
10. To study RC low pass filter and measurement of cut-off frequency from graph.
11. To shift RC High pass Filter.
12. To study the application of Superposition theorem.