Kurukshetra University, Kurukshetra

(Established by the State Legislature Act XII of 1956)
('A+' Grade, NAAC Accredited)

।। योगस्थः कुरु कर्माणि।।
समबुद्धि व योग युक्त होकर कर्म करो

(Perform Actions while Stead fasting in the State of Yoga)

DEPARTMENT OF ELECTRONIC SCINENCE

CBCS CURRICULUM (2020 -21)
Program Name: M. Tech.-Microelectronics and VLSI Design
(For the Batches Admitted From 2020-2021)

OUTCOME BASED EDUCATION SYSTEM

CBCS CURRICULUM (2020-21)

Program Name: M. Tech.-Microelectronics and VLSI Design
(For the Batches Admitted From 2020-21)

VISION

Be globally acknowledged as a distinguished centre of academic excellence.

MISSION

To prepare a class of proficient scholars and professionals with ingrained human values and commitment to expand the frontiers of knowledge for the advancement of society.

DEPARTMENT VISION AND MISSION

VISION

- To become a model department as a Centre of quality education, research with innovation and recognition at National and International level for serving society.

MISSION

- M1: To provide quality education to aspiring young minds for improving their scientific knowledge and technical skills in the area of Electronic Science.
- M2: To produce socially committed trained professionals who can contribute effectively to the advancement of their organization and society through their scientific knowledge.
- M3: To foster innovation in Electronic Science and allied areas by collaborating with industry and other R& D organizations.

Mapping of University Vision and Mission to Department Vision and Mission

Acclaimed as centre of academic excellence and collaborative research by

University Vision and Mission	Department Vision and Mission
High quality knowledge delivery through state of art infrastructure and ethical values to the students	**Yes**
Students excellence will make them professionals and innovators emerging as global leaders	**Yes**
Research and development will help in furtherance of Faculty knowledge	**Yes**

Programme Educational Objectives (PEOs):

The Department of Electronic Science in consultation with various stakeholders have formulated the Programme Educational Objectives (PEO's). These PEO's of the M. Tech.

Microelectronics and VLSI Design programme are as follows:

- **PEO1:** To train the students to make them capable of exploiting and enhancing theoretical and practical knowledge in domains of Microelectronics and VLSI Design.

- **PEO2:** Students are trained to develop practical and efficient solutions to the challenges of designing and generating GDS files for digital, analog and mixed signal integrated circuits using appropriate EDA tools, computational techniques, and algorithms.

- **PEO3:** To perceive lifelong learning as a means of enhancing knowledge base and skills necessary to become a successful professional or entrepreneur in the domain and contribute towards the growth of community as well as society.

Program Specific Outcomes (PSO's):

PSO1: Ability to use the techniques, skills, and modern VLSI Design tools necessary for Electronic System Designs.

PSO2: Ability to apply the knowledge of electronics to design and implement complex VLSI systems.

PSO3: Ability to design and conduct experiments based on Microelectronics & VLSI, as well as to analyze and interpret data.

PEOs to Mission statement mapping

PEO's	MISSION OF THE DEPARTMENT		
	M1	M2	M3
PEO1	3	3	1
PEO2	2	3	2
PEO3	1	2	3

Program Outcomes (PO) with Graduate Attributes

The Graduate Attributes are identified by National Board of Accreditation. The Programme Outcomes are attributes of the graduates from the programme that indicates the graduates' ability and competence to work and the skills as well that the students acquire from the programme. Program Outcomes are statements that describe what students are expected to know or do by the time of graduation, they must relate to knowledge and skills that the students acquire from the programme. The achievement of all outcomes indicates that the student is well prepared to achieve the program educational objectives down the road. The course syllabi and the overall curriculum are designed to achieve the following outcomes during M.Tech in Microelectronics and VLSI Design:

S. No	Graduate Attributes	Program Outcomes (POs)
1	Knowledge	**PO1**: Capability of demonstrating comprehensive disciplinary knowledge gained during course of' study

2	Research Aptitude	**PO2:** Capability to ask relevant/appropriate questions for identifying, formulating and analyzing the research problems and to draw conclusion from the analysis.
3	Communication	**PO3:** Ability to communicate effectively on general and scientific topics with the scientific community and with society at large
4	Problem Solving	**PO4:** Capability of applying knowledge to solve scientific and other problems
5	Individual and Team Work	**PO5:** Capable to learn and work effectively as an individual, and as a member or leader in diverse teams, in multidisciplinary settings.
6	Investigation of Problems	**PO6**: Ability of critical thinking, analytical reasoning and research based knowledge including design of experiments, analysis and interpretation of data to provide conclusions
7	Modern Tool Design	**PO7:** ability to use and learn techniques, skills and modern tools for scientific practices
8	Science and Society	**PO8:** Ability to apply reasoning to assess the different issues related to society and the consequent responsibilities relevant to professional scientific practices
9	Life-Long Learning	**PO9:** Aptitude to apply knowledge and skills that are necessary for participating in learning activities throughout life.
10	Ethics	**PO10:** Capability to identify and apply ethical issues related to one's work; avoid unethical behavior such as fabrication of data, committing plagiarism and unbiased truthful actions in all aspects of work.
11	Project Management	**PO11:** Ability to demonstrate knowledge and understanding of the scientific principles and apply these to manage projects.

Mapping of PEO's with PO's

S. No.	*Program Educational Objectives*	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
1	To train the students to make them capable of exploiting and enhancing theoretical and practical knowledge in domains of Microelectronics and VLSI Design.	√	√	√	√		√	√		√		√	√	√	√
2	Students are trained to develop practical and efficient solutions to the challenges of designing and generating GDS files for digital, analog and mixed signal integrated circuits using appropriate EDA tools, computational techniques, and algorithms.	√	√			√	√			√	√		√	√	√
3	To perceive lifelong learning as a means of enhancing knowledge base and skills necessary to become a successful professional or entrepreneur in the domain and contribute towards the growth of community as well as society.			√	√		√	√	√	√	√	√	√	√	

Kurukshetra University, Kurukshetra

Scheme of Examination & Syllabus of M.Tech. (Microelectronics & VLSI Design) (CBCS)
(I to IV Semesters) w.e.f. Session 2020-2021 (in phased manner)

Course	Name of the Subject	Workload Hours per week	Hours/ Week Credit		Internal Assessment Marks	Exam/ Practical Marks	Total Credits	Duration of Exam
			L	P				
	I Semester							
MMVD 101	Process Technology for ULSI –I	4	4	0	40	60	4	3 Hrs.
MMVD 102	MOSFET Physics and Sub-Micron Device Modeling	4	4	0	40	60	4	3 Hrs.
MMVD 103	VLSI Design	4	4	0	40	60	4	3 Hrs.
MMVD 104	Digital Signal Processing	4	4	0	40	60	4	3 Hrs.
MMVD 105	Lab Work – I	16	0	8	40	60	8	4 Hrs.
					200	300		
			Total		500		24	
	II Semester							
MMVD 201	Process Technology for ULSI –II	4	4	0	40	60	4	3 Hrs.
MMVD 202	Embedded System Design using 8051	4	4	0	40	60	4	3 Hrs.
MMVD 203	Analog CMOS Integrated Circuits	4	4	0	40	60	4	3 Hrs.
MMVD 204	Verilog - Hardware Description Language	4	4	0	40	60	4	3 Hrs.
MMVD 205	Lab Work – II	16	0	8	40	60	8	4 Hrs.
					200	300		
			Total		500		24	
	III Semester							
MMVD 301	Program Elective-I*	4	4	0	40	60	4	3 Hrs.
MMVD 302	Program Electives-I*	4	4	0	40	60	4	3 Hrs.
MMVD 303	Program Electives-I*	4	4	0	40	60	4	3 Hrs.
MMVD 304	Minor Project**	16	0	8	0	100	8	4 Hrs.
					120	280		
			Total		400		20	
	IV Semester							
MMVD 401	Project Dissertation - Evaluation & Viva Voce **		0	0	0	300	20	
			Total				20	

***For each of the following three courses student can opt any one subject from Program Elective I or Program Elective II.**

Course	Program Elective – I	Program Elective – II
MMVD 301	Micro Electro Mechanical Systems (MEMS)	RF Microelectronics
MMVD 302	Embedded System Design using ARM	Digital System Testing and Fault Simulation
MMVD 303	Nano Science & Technology	Digital Signal Processing in VLSI

* Note: Minor project will be a kind of open ended problem based project. Topic/Title will be chosen by the students in the relevance of the studied courses during M.Tech.(MMVD). The evaluation for Minor Project will be based on the presentation /Viva-Voce given by student to examiners appointed by the PG Board of studies.

** Note: The Project is to be carried out for sic month during Jan-June in an Industry or Institute of repute or in the Department labs. The students are required to submit a dissertation. Evaluation will be done by examiners appointed by the PG Board of studies and will be based on the dissertation and Viva-Voce. These will be acceptance with grades (grade 'A', grade 'B' and Grade 'C') or rejection of project thesis.
In theory papers, the internal assessment will be based on two class tests, one assignment and attendance in the class as per the classification given in academic ordinance for M.Tech. Courses. Where two teachers are teaching the subject, average of the tests and assignments will be considered.

CBCS CURRICULUM (2020 -21)
Program Name: M. Tech (Microelectronics and VLSI Design)

Course Code: MMVD 101	**Course Name:** Process Technology for ULSI – I	**L**	**T**	**P**	**C**
		4	**0**	**0**	**4**
Year and Semester	**1st Year** **1st Semester**	**Contact hours per week:** (4 Hrs.) Exam: (3 Hrs.)			
Pre-requisite of course	**NIL**	**Evaluation**			
		Internal Assessment: 40	**Theory Examination: 60**		

Course Objectives:

1. To learn the concepts of clean room environment for Fabrication of integrated circuits.
2. To understand the theory and concept of cleaning process for silicon and other wafers for IC fabrication
3. To develop skills for simulating the various fabrication processes.
4. To understand the process integration flow for different IC fabrication technologies.

Course Outcomes:

CO1	Describe the requirements of cleanrooms for IC fabrication
CO2	Implement the Silicon wafer cleaning process for device fabrication.
CO3	Design and simulate the fabrication processes required for IC fabrication.
CO4	Explain process integration flow for different IC fabrication technologies.

Mapping of Course Outcomes to Program Outcomes:

CO's	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3	3	2	2	2	3	3	2	3	--	--	2	2	2
CO2	3	3	2	3	2	3	3	2	2	--	--	3	2	3
CO3	3	3	2	3	3	3	3	3	2	--	2	3	3	3
CO4	3	3	3	2	3	3	3	3	3	--	2	3	3	3

CONTENTS	**Hrs.**	**COs**
Unit I Clean Room Technology, Clean Room Classifications, Design concepts, Clean Room Installations and Operations, Automation related facility systems, future trends.	**8**	**CO1**
Unit II Wafer Cleaning Technology - Basic Concepts, Wet cleaning, Dry cleaning, Epitaxy, Fundamental Aspects, Conventional silicon epitaxy, low temperature, Epitaxy of silicon, selective epitaxial growth of Si, Characterization of epitaxial films.	**10**	**CO2** **CO3**

Unit III Process simulation, Introduction, Ion-implantation, Monte Carlo method, Diffusion and Oxidation, two-dimensional LOCOS simulation example, Epitaxy, Epitaxial doping model, Lithography, Optical projection lithography, Electron-beam lithography, Etching and deposition, future trends.	**11**	**CO3**
Unit IV VLSI Process Integration, Fundamental considerations for IC Processing, building individual layer, integrating the process steps, miniaturizing VLSI circuits, NMOS IC technology, fabrication process sequence, special consideration for NMOS ICs, CMOS IC technology, Fabrication Process sequence, special considerations for CMOS ICs, MOS memory IC technology, dynamic memory, static memory, bipolar IC technology, fabrication process sequence, special considerations for bipolar ICs, Self-aligned bipolar structures, Integrated injection logic, IC fabrication, process monitoring future trends.	**11**	**CO4**

Reference:

1. VLSI Technology by S.M.Sze.
2. ULSI Technology by C.Y. Chang and S.M. Sze (McGraw Hill International)

Note for Examiner(s):

There are eight questions in all organized in four sections and each section is having two questions from each of the four units. The candidate shall have to attempt five questions in all, selecting at least one question from each unit.

Assessment Pattern:

Outcomes	**Internal Evaluation (40 Marks)**				**Semester End Examination (60 Marks)**
	Test1	**Test2**	**Test 3**	**Assignment(5)+Attendance(5)**	**SEE**
Marks	**15**	**15**	**15**	**10**	**60**
CO1	15	--	--	--	15
CO2	--	15	--	--	15
CO3	--	--	10	--	15
CO4	--	--	5	5	15

Course Code: MMVD 102	**Course Name:** MOSFET Physics and Sub-Micron Device Modeling	**L**	**T**	**P**	**C**
		4	**0**	**0**	**4**

Year and Semester	**1st Year** **1st Semester**	**Contact hours per week:** (4 Hrs.) Exam: (3 Hrs.)	
Pre-requisite of course	**NIL**	**Evaluation**	
		Internal Assessment: 40	**Theory Examination: 60**

Course Objectives:

1. To learn the concepts of semiconductor electronic properties based on energy band structure
2. To analyse the significance of electron and hole concentrations and Fermi level in semiconductors.
3. To develop skills for constructing energy band diagrams for semiconductor structures and devices.
4. To learn I-V and C-V characteristics of MOS.
5. To learn second order effects in MOSFET
6. To learn about the Nonconventional MOSFET devices
7. To learn the EDA tools to understand the second order effects.

Course Outcomes:

CO1	Understand the physics of semiconductors devices.
CO2	Analyze the different parameters responsible for the performance of a semiconductor device.
CO3	Differentiate the conduction mechanism of semiconductor devices based upon their energy band diagram.
CO4	Extract the parameters from the I-V and C-V characteristic curves of MOS device.
CO5	Understand the second order effects in MOSFET
CO6	Differentiate the working of different Non-conventional MOS devices
CO7	Simulate the second order effects in MOSFET devices.

Mapping of Course Outcomes to Program Outcomes:

CO's	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3	3	3	2	2	3	3	2	2	--	--	2	2	2
CO2	3	3	2	3	2	3	3	2	3	--	--	3	2	3
CO3	3	3	2	2	3	3	3	3	2	--	--	3	3	3
CO4	3	3	3	3	3	3	3	2	3			3	3	3
CO5	3	3	2	3		3	3	3	3	--	--	3	2	3
CO6	3	3	3		3		3	3	3	--	--	3	2	3
CO7	3	3	3	2	3	3	3	3	3	--	--	2	3	3

CONTENTS	Hrs.	COs
Unit I Metal Semiconductor contacts – idealized Metal, Semiconductor junction, current voltage characteristics of schottky barrier, ohmic contacts, surface effects, MOS electronics, capacitance of the MOS system, non-ideal MOS system. Basic MOSFET behavior, Channel length modulation, Body bias effect, Threshold voltage adjustment,Sub threshold conduction.	**10**	**CO1 CO2**
Unit II Limitation of long channel analysis, short channel effects, mobility degradation, velocity saturation, drain current in short channel MOSFETS, MOSFET scaling and short channel model, CMOS devices, MOSFET scaling goals , gate coupling, velocity overshoot, high field effects in scaled MOSFETs, substrate current, hot carrier effects, effects of substrate current on drain current, gate current in scaled MOSFETS.	**10**	**CO2 CO3 CO4**
Unit III Moore law, Technology nodes and ITRS, Physical & Technological Challenges to scaling, Nonconventional MOSFET – (FDSOI, SOI, Multi-gate MOSFETs).	**10**	**CO6**
Unit IV Numerical Simulation, basic concepts of simulations, grids, device simulation and challenges. Importance of Semiconductor Device Simulators - Key Elements of Physical Device Simulation, Historical Development of the Physical Device Modeling.Introduction to the Silvaco ATLAS Simulation Tool, Examples of Silvaco ATLAS Simulations – MOSFETs and SOI.	**10**	**CO5 CO7**

Reference:

1. Device Electronics for Integrated circuits by Muller and Kammins.
2. Computational Electronics by DragicaVasileska and Stephen M. Goodnick.
3. Silicon Nanoelectronics – Shundri Oda & David Ferry, CRC Press

Note for Examiner(s):

There are eight questions in all organized in four sections and each section is having two questions from each of the four units. The candidate shall have to attempt five questions in all, selecting at least one question from each unit.

Assessment Pattern:

Outcomes	Internal Evaluation (40 Marks)				Semester End Examination (60 Marks)
	Test1	Test2	Test 3	Assignment(5)+Attendance(5)	SEE
Marks	**15**	**15**	**15**	**10**	**60**
CO1	10	--	--	--	5
CO2	5	5	--	--	10
CO3	--	5	--	--	5
CO4	--	5	--	5	10
CO5			5		10
CO6			5		10
CO7			5		10

Course Code: MMVD 103	**Course Name:** VLSI Design	**L**	**T**	**P**	**C**
		4	**0**	**0**	**4**
Year and Semester	**1st Year** **1st Semester**	**Contact hours per week:** (4 Hrs.) Exam: (3 Hrs.)			
Pre-requisite of course	**NIL**	**Evaluation**			
		Internal Assessment: 40	**Theory Examination: 60**		

Course Objectives:

1. To Understand design methodologies and techniques applicable to VLSI technology.
2. Ability to design logic circuit layouts for both static CMOS and dynamic clocked CMOS circuits
3. Advance the knowledge and understanding of current developments in VLSI technology

Course Outcomes:

CO1	Design CMOS inverters with specified noise margin and propagation delay.
CO2	Design and optimize the combinational logic and sequential logic as well.
CO3	Implement efficient techniques at circuit level for improving power and speed of combinational and sequential circuits.
CO4	Design and optimize Sub-systems.

Mapping of Course Outcomes to Program Outcomes:

CO's	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3	1	1	3	2	2	3		2	--	--	3	3	2
CO2	3	2	1	3	2	2	3		2	--	--	3	3	2
CO3	3	3	1	3	2	2	3		2	--	--	3	3	2
CO4	3	3	1	3	2	2	2		2	--	--	3	3	2

CONTENTS	**Hrs.**	**COs**
Unit I Transistors and layouts - Transistors, Wires and Vias, Design Rules, Layout Design and Stick Diagrams - example, Logic Gate – Pseudo NMOS, DCVS, Domino. Delay through Resistive Interconnect. CMOS Inverter: Basic Circuit and DC Operation – DC Characteristics.	**11**	**CO1**
Unit II Inverter Switching Characteristics- Static behavior– Switching threshold, Noise Margin, CMOS Inverter Dynamic Behavior- capacitances, propagation delay - High-to-Low time, Low to High time, Sources of Power Consumption, Power Consumption Static and dynamic. Logic Gate - Switch Logic.	**10**	**CO3**

Unit III Combinational Logic Design- Standard cell based layout, CMOS Logic Circuits – CMOS NOR, NAND, Combinational network delays – Fan out, path delay, transistor sizing, cross talk minimization, power optimization. CMOS Transmission Gate (Pass gates). Sequential Logic design – Setup and hold time, SR latch circuit, clocked latch and flip flop circuits.	**10**	**CO2**
Unit IV Sub system design, Design Principles, Adders, ALUs, High Density Memory, ROM, Static RAM case study of 4-M bit SRAM. FPGAs, PLAs. Floor Planning, Methods of Floor Planning, Chip Connections.	**9**	**CO4**

References:

1. Modern VLSI Design Systems on Silicon by Wayne Wolf (Pearson Education Asia)
2. CMOS Digital Integrated circuits- Analysis and design by Sung- Mo Kang and Yusuf Leblenici - MGH
3. Digital Integreted Circuits-(A design perspective) Jan M. Rabaey-P.M.I
4. Basic VLSI design-(Systems and Units (2nd edition) Pucknell & Eshraghian (PHI)
5. CMOS/BiCMOS VLSI by Yeo (Pearson).

Note for Examiner(s):

There are eight questions in all organized in four sections and each section is having two questions from each of the four units. The candidate shall have to attempt five questions in all, selecting at least one question from each unit.

Assessment Pattern:

Outcomes	**Internal Evaluation (40 Marks)**				**Semester End Examination (60 Marks)**
	Test1	**Test2**	**Test 3**	**Assignment(5)+Attendance(5)**	**SEE**
Marks	**15**	**15**	**15**	**10**	**60**
CO1	10	--	--	--	15
CO2	5	10	--	--	15
CO3	--	5	10	--	15
CO4	--	--	5	5	15

Course Code: MMVD 104	**Course Name:** Digital Signal Processing	**L**	**T**	**P**	**C**
		4	**0**	**0**	**4**
Year and Semester	**1st Year** **1st Semester**	**Contact hours per week:** (4 Hrs.) Exam: (3 Hrs.)			
Pre-requisite of course	**NIL**	**Evaluation**			
		Internal Assessment: 40	**Theory Examination: 60**		

Course Objectives:

1. To learn the basic of Characterization and Classification of signals.
2. To understand the concept of typical signals, Typical signal Processing applications, Digital Signal Processing requirements.
3. To understand the Discrete time signals and systems and Time domain characterization of LTI Discrete- time systems
4. To develop skills for to compute the z-transform of a sequence, identify its region of convergence, and compute the inverse z-transform.
5. To understand the concept and fundamentals of didgital filter design

Course Outcomes: On completion of the course, student would be able to:

CO1	Understand the basic of Characterization and Classification of signals.
CO2	Understand Significance of DSP through practical life examples.
CO3	Compute the linear convolution of two sequences using DFT.
CO4	Compute the z-transform of a sequence, identify its region of convergence, and compute the inverse z-transform by partial fractions.
CO5	Understand the fundamentals of digital filter design.

Mapping of Course Outcomes to Program Outcomes:

CO's	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3	3	3	2	2	3	3	2	2	--	--	2	2	2
CO2	3	3	2	3	2	3	3	2	2	--	--	3	2	2
CO3	3	3	3	2	3	3	2	2	2	--	--	3	3	2
CO4	3	3	2	2	2	3	3	2	2	--	--	2	2	2
CO5	3	3	3	2	2	3	3	2	2	--	--	2	2	2

CONTENTS	**Hrs.**	**COs**
Unit I Characterization and Classification of signals, typical signal processing operation. Examples of typical signals, Typical signal Processing Applications, Need of Digital Signal Processing.	**10**	**CO1** **CO2**

Unit II Time Domain Representation of Signals and System- Discrete time signals, Operation on sequences, Discrete time systems, Time domain characterization of LTI Discrete- time systems, State-space Representation of LTI Discrete Time Systems.	**10**	**CO3**
Unit III The Discrete-Time Fourier Transform, Discrete Fourier Transform, Discrete Fourier Transform Properties, The z-transform, The inverse z-transform, Properties of z transform, Transform Domain Representations of LTI Systems- The frequency Response, transfer function.	**10**	**CO4**
Unit IV Digital Filter Structure- Block diagram Representation, signal-flow-graph representation, equivalent structures, Basic FIR Digital Filter Structures, Basic IIR Filter structures. Digital Filter Design- Low Pass IIR Digital Filter Design Examples	**10**	**CO4** **CO5**

References:

1. Digital Signal Processing by Sanjit K.Mitra (TMH)
2. Digital Signal Processing by S. Salivahanan, A. Vallavaraj, Tata McGraw-Hill.
3. Digital Signal Processing by John G. Prokais and Dimitris K Manolakis (Pearson)
4. Introduction to Digital Signal Processing by Johnson (PHI)
5. Digital Signal Processing: Theory, Analysis and Digital Filter Design by Nair (PHI)

Note for Examiner(s):

There are eight questions in all organized in four sections and each section is having two questions from each of the four units. The candidate shall have to attempt five questions in all, selecting at least one question from each unit.

Assessment Pattern:

Outcomes	**Internal Evaluation (40 Marks)**				**Semester End Examination (60 Marks)**
	Test1	**Test2**	**Test 3**	**Assignment(5)+Attendance(5)**	**SEE**
Marks	**15**	**15**	**15**	**10**	**60**
CO1	10	--	--	--	10
CO2	5	--	--	--	5
CO3	--	15	--	--	15
CO4	--	--	10	5	15
CO5			5		15

Course Code: MMVD 105	**Course Name:** Lab Work I	**L**	**T**	**P**	**C**
		0	**0**	**16**	**8**

Year and Semester	**1st Year** **1st Semester**	**Contact hours per week:** (16 Hrs.) Exam: (4 Hrs.)	
Pre-requisite of course	**NIL**	**Evaluation**	
		Internal Assessment: 40	**Theory Examination: 60**

Course Objective:

1. To do hands-on on the cleaning of silicon wafers and physical vapor deposition of various metals on substrates.
2. To simulate the processes involved in fabrication of MOSFET.
3. To design and TCAD simulation of MOSFET at circuit level.
4. To learn basics of LINUX and C programming.
5. To develop the skills for MATLAB coding and simulation of various digital signal processes.
6. To do basic analog circuit simulation using P-SPICE.

Course Outcomes:

CO1	Understand the fundamental concepts of Linux.
CO2	Apply the basic programming skills of C Language in problem solving.
CO3	Simulate various fabrication processes involved in MOSFET.
CO4	Design and simulate MOSFET at circuit level using TCAD tool.
CO5	Apply basic programming skills of MATLAB for solving DSP problems.
CO6	Analog circuit simulation using P-SPICE.

Mapping of Course Outcomes to Program Outcomes:

CO's	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3	3	2	2	2	3	2	2	2	3	1	3	3	3
CO2	3	3	2	3	2	3	2	2	2	3	1	3	3	3
CO3	3	3	2	3	2	2	3	2	3	2	1	3	3	3
CO4	3	3	2	2	3	2	3	2	3	2	1	3	3	3
CO5	3	3	2	2	3	3	3	2	2	2	1	3	3	3
CO6	3	3	2	2	2	3	3	2	2	2	1	3	3	3

Course Contents:

Perform all of the following experiments:

1. Cleaning and testing of silicon wafer and Metallization for contacts and interconnects.
2. Design & Process Simulation of MOSFET using Athena.
3. Design and simulation of MOSFET inverters using VTCAD.
4. Familiarizations with basic Linux commands using Linux prompt, C Programming.
5. Digital signal processing experiments
   (I). Represent basic signals (unit step, unit impulse, ramp, sine, cosine and exponential) using MATLAB
   (II) Write a program for discrete convolution
   (III) Write a program for sampling theorem
   (IV) To design the digital low pass IIR filters
6. Circuit simulation using P-SPICE

Course Code: MMVD 201	**Course Name:** Process Technology for ULSI-II	**L**	**T**	**P**	**C**
		4	**0**	**0**	**4**

Year and Semester	**1st Year** **2nd Semester**	**Contact hours per week:** (4 Hrs.) Exam: (3 Hrs.)	
Pre-requisite of course	**NIL**	**Evaluation**	
		Internal Assessment: 40	**Theory Examination: 60**

Course Objective:

1. To learn the concepts of Rapid thermal processes.
2. To understand different technologies for thin film deposition.
3. To understand various lithographic techniques.
4. To learn the concept of etching and understand different material etching techniques.
5. To learn metallization techniques for interconnections.
6. To understand various MOS technologies like BICMOS and MOS memory technology.
7. To learn process integration and IC packaging.

Course Outcomes: On completion of the course, student would be able to:

CO1	Describe the difference between the furnace processes and the rapid thermal processes.
CO2	Describe the advantages and disadvantages between various thin film techniques.
CO3	Find out the significance of lithographic techniques like optical lithography, e-beam lithography, x-ray lithography and ion- beam lithography.
CO4	Understand the significance of different etching techniques for device fabrication.
CO5	Analyse the role of metallization to optimize the RC delay during interconnections on the chip.
CO6	Understand different MOS technologies.
CO7	Describe the role of assembly and packaging in IC fabrication.

Mapping of Course Outcomes to Program Outcomes:

CO's	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3	2	2	2	3	3	3	3	2	--	3	2	2	2
CO2	3	3	2	2	2	3	3	2	3	--	3	3	2	3
CO3	3	3	2	3	2	3	3	3	2	--	--	3	3	3
CO4	3	3	3	3	3	3	3	2	2	--	--	2	3	3
CO5	3	2	3	3	2	3	2	3	2	--	--	3	2	3
CO6	3	2	3	2	3	3	3	3	2	--	--	3	3	3
CO7	3	3	2	3	3	3	3	3	3	--	--	2	3	2

CONTENTS	Hrs.	COs
Unit I Conventional Rapid thermal processes, Requirement for thermal processes, Rapid thermal processes, Future trends. Dielectric and Poly silicon film deposition processes, Atmospheric pressure CVD and low pressure CVD based silicon oxide, LPCVD Silicon Nitrides, LPCVD Poly Si Films, Plasma assisted depositions.	**10**	**CO1 CO2**
Unit II Other deposition methods, Applications of deposited poly Silicon, Silicon oxide and Silicon nitride films.Lithography, Optical, Electron, X-Ray, Ion lithographies.	**10**	**CO2 CO3**
Unit III Etching, Low pressure gas discharge, etch mechanism, selectivity and profile control, Reactive plasma etching techniques and equipment, Plasma based processes, diagnostics and point control and damage, wet chemical etching. Metallization, Metal deposition techniques, Silicide Process.	**10**	**CO4 CO5**
Unit IV CVD Tungsten Plug, Other plug processes, Multi level metallization, Metallization Reliability. Process Integration, Bi CMOS technology, MOS Memory technology, Process Integration Considerations. Assembly and packaging: introduction.	**10**	**CO6 CO7**

Reference:

1. ULSI Technology by C.Y. Chang and S. M. Sze (McGraw Hill International)

Note for Examiner(s):

There are eight questions in all organized in four sections and each section is having two questions from each of the four units. The candidate shall have to attempt five questions in all, selecting at least one question from each unit.

Assessment Pattern:

Outcomes	Internal Evaluation (40 Marks)				Semester End Examination (60 Marks)
	Test1	Test2	Test 3	Assignment(5)+Attendance(5)	SEE
Marks	**15**	**15**	**15**	**10**	**60**
CO1	10	--	--	--	5
CO2	5	5	--	--	10
CO3	--	10	--	--	10
CO4	--	--	--	5	5
CO5	--	--	--	--	10
CO6	--	--	5	--	10
CO7	--	--	10	--	10

Course Code: MMVD 202	**Course Name:** Embedded System Design using 8051	**L**	**T**	**P**	**C**
		4	**0**	**0**	**4**
Year and Semester	**1st Year** **2nd Semester**	**Contact hours per week:** (4 Hrs.) Exam: (3 Hrs.)			
Pre-requisite of course	**NIL**	**Evaluation**			
		Internal Assessment: 40	**Theory Examination: 60**		

Course Objective:

1. To familiarize with need and application of embedded system.
2. To understand the architecture, operation and programming of 8051.
3. To understand the design, parameters and constraints of embedded system.

Course Outcomes: On completion of the course, student would be able to:

CO1	Understand the basic of Embedded Design, RISC and CISC Operation.
CO2	Apply the basic programming skills of 8051 in problem solving.
CO3	Understand RTOS – basics and its relevance in embedded system.

Mapping of Course Outcomes to Program Outcomes:

CO's	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3	3	2	2	3	3	3	1	2	--	2	2	2	2
CO2	3	3	2	2	3	3	3	2	2	--	2	3	2	3
CO3	3	3	2	2	3	3	3	1	2	--	2	3	3	3

CONTENTS	**Hrs.**	**COs**
Unit I Embedded systems – introduction, role of processor and other hardware units, real-life examples, embedded systems on chip, Introduction to CISC and RISC architecture. Structural units of processor, processes selection for embedded system, memory devices for embedded systems and allocation of memory, DMA, interfacing memory, processor and I/O devices.	**10**	**CO1**
Unit II Devices for embedded systems: I/O devices, timer and counting devices, Microprocessor and Micro controllers: differences, 8-bit micro controllers - comparison. Types of microcontrollers.The 8051 architecture: microcontroller hardware, I/O pins, ports and circuit, external memory, counter & timer, serial data input/output, interrupts.	**10**	**CO1** **CO2**
Unit III Programming of 8051 – instruction syntax, addressing modes, external data moves, code memory read-only data moves, push and pop opcodes, data exchange, logical operations, arithmetic operation, jump and call instructions. Case studies: pulse generator/ PWM, Digital Lock, Stepper motor control.	**10**	**CO2**

Unit IV Real word interfacing with 8051: external memory, 8255, ADC, DAC. RTOS – basics and relevance in embedded system, typical applications hardware – software co-design in an embedded system: project management, design and co-design issues in system development process, design cycle, emulator and in-circuit emulator (ICE), use of software tools for development of an embedded system, issuers in embedded system design.	**10**	**CO3**

References:

1. Raj Kamal, Embedded Systems, Architecture, Programming and Design, TMH, 2003
2. The 8051 microcontroller – by Ayala (Penram)
3. Programming and Customizing the 8051 Microcontroller by Predko, Myke,, TMH, 2003
4. The 8051 MicroController& Embedded systems by MA. Mazidi & JG. Mazidi(Pearson)
5. Designing Embedded H/W By John Catsoulis (O'Reilly)

Note for Examiner(s):

There are eight questions in all organized in four sections and each section is having two questions from each of the four units. The candidate shall have to attempt five questions in all, selecting at least one question from each unit.

Assessment Pattern:

Outcomes	**Internal Evaluation (40 Marks)**				**Semester End Examination (60 Marks)**
	Test1	**Test2**	**Test 3**	**Assignment(5)+Attendance(5)**	**SEE**
Marks	**15**	**15**	**15**	**10**	**60**
CO1	15	5	--	--	15
CO2	--	10	--	--	25
CO3	--	--	15	5	20

.

Course Code: MMVD 203	**Course Name:** Analog CMOS Integrated Circuits	**L**	**T**	**P**	**C**
		4	**0**	**0**	**4**

Year and Semester	**1st Year** **2nd Semester**	**Contact hours per week:** (4 Hrs.) Exam: (3 Hrs.)	
Pre-requisite of course	**NIL**	**Evaluation**	
		Internal Assessment: 40	**Theory Examination: 60**

Course Objective:

1. To understand the operation of CMOS devices, familiar with the small- and large-signal models of CMOS transistors.
2. Analyze the basic current mirrors, understanding the voltage references, analyze and design basic operational amplifiers.
3. To understand the concept of gain, power, and bandwidth, design basic circuits using EDA tools.
4. To understand the Switched capacitor circuits and data converters.

Course Outcomes:

CO1	Understand the significance of different biasing styles and apply them aptly for different circuits.
CO2	Design basic building blocks like sources, sinks, mirrors.
CO3	To Comprehend the stability issues of the systems.
CO4	Design OpAmp fully compensated against process, supply and temperature variations.
CO5	Design Analog integrated system including parasitic effects.
CO6	Analyze Switched Capacitor Circuits and data converters.

Mapping of Course Outcomes to Program Outcomes:

CO's	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3	3		2		3	2	3	1			3	3	3
CO2	3	3		2		3	2	3	1			3	3	3
CO3	3	2		3		3	2	2	1			3	3	3
CO4	3	2		3		3	2	2	1			3	3	3
CO5	3	3		2		3	2	2	1			3	3	3
CO6	3	3		2		3	2	2	1			3	3	3

CONTENTS	**Hrs.**	**COs**
Unit I Introduction to analog design, Why analog, why CMOS ,Levels of abstraction, Robust analog design, MOS models, long channel vs short channel, Analog layout, short channel considerations, Matching, Resistor layout, Noise considerations, Latchup.	**10**	**CO1** **CO3**

Unit II Single stage amplifier, Basic concepts, Common source stage, Source follower, common gate stage. Band gap reference: General considerations, Supply independent biasing, temperature-independent references, negative-TC voltage, positive TC voltage, PTAT generation Folded cascode, Differential amplifiers, Single ended and differential operation, common mode response Differential pair with MOS loads, Gilbert Cell.	**10**	**CO1** **CO2**
Unit III Current mirror, Cascode Current mirrors, Active Current mirror, Operational Amplifiers, One stage and two stage Op Amps, Gain boosting, Comparison, Common-mode Feedback, Input Range limitations, stability and frequency compensations, Comparator using OPAMPs (brief).	**10**	**CO4** **CO5**
Unit IV Switched capacitor circuits, Basic operation and analysis, switched Capacitor Gain Circuits; Data Converter fundamentals, Ideal D/A converter, Quantization noise, signed codes, performance limitations.	**10**	**CO6**

References:

1. Analog integrated circuit Design, David A. Johns & Ken Martin - John- Wiley &Sons, Inc. New York.
2. Design of Analog CMOS integrated circuits Behzad Razavi McGraw-Hill International edition.
3. CMOS: Circuit Design, layout, and simulation, R. Jacob, Baker and David E. Boyce, Prentice Hall of India.
4. Applications and Design with analog integrated circuits, 2 nd Edition - J. Michael Jacob, Prentice Hall of India.
5. Design and applications of analog Integrated Circuits, Prentice Hall of India,

Note for Examiner(s):

There are eight questions in all organized in four sections and each section is having two questions from each of the four units. The candidate shall have to attempt five questions in all, selecting at least one question from each unit.

Outcomes	**Internal Evaluation (40 Marks)**				**Semester End Examination (60 Marks)**
	Test1	**Test2**	**Test 3**	**Assignment(5)+Attendance(5)**	**SEE**
Marks	**15**	**15**	**15**	**10**	**60**
CO1	5	--	--	--	5
CO2	10		--	--	10
CO3	--	5	--	--	10
CO4	--	10	--	--	15
CO5	--		5	5	10
CO6	--	--	10	--	10

Course Code: MMVD 204	**Course Name:** Verilog - Hardware Description Language	**L**	**T**	**P**	**C**
		4	**0**	**0**	**4**
Year and Semester	**1st Year** **2nd Semester**	**Contact hours per week:** (4 Hrs.) Exam: (3 Hrs.)			
Pre-requisite of course	**NIL**	**Evaluation**			
		Internal Assessment: 40	**Theory Examination: 60**		

Course Objective:

1. To Design state machines to control complex systems.
2. Define and describe digital design flows for system design and recognize the trade-offs involved in different approaches.
3. To write synthesizable Verilog code and a Verilog test bench to test Verilog modules.
4. To Analyze code coverage of a Verilog test bench and debug Verilog modules.
5. Target a Verilog design to an FPGA board

Course Outcomes:

CO1	Understand the fundamentals of Verilog HDL and its need in Digital design.
CO2	To design and write synthesizable Verilog HDL codes, and also its test bench.
CO3	Design the state machines for specific problems and implement it on FPGA board.
CO4	Design combinational and sequential circuits using Verilog HDL.

Mapping of Course Outcomes to Program Outcomes:

CO's	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3		2	2		3	3		2			3	3	2
CO2	3		2	2		3	3		2			3	3	2
CO3	3		2	2		3	3		2			3	3	2
CO4	3		2	2		3	3		2			3	3	2

CONTENTS	**Hrs.**	**COs**
Unit I Verilog: Overview of Digital Design with Verilog HDL, Hierarchical Modeling, Basics of Verilog - Data Types, System Tasks and Compiler Directives, Modules and Ports, Gate Level Modeling- Gate Types, Gate Delays.	**10**	**CO1** **CO2**
Unit II Behavioral Modeling - Structured Procedures, Procedural Assignments, Timing Controls, Conditional Statements, Multiway Branching, Loops, Sequential and Parallel Blocks, Tasks and Functions – Exercises. FSM based HDL design-Moore & Mealy machines.	**10**	**CO2** **CO3** **CO4**

Unit III Useful modeling techniques- Procedural continuous assignments, overriding parameters, conditional compilation and execution, time scales, useful system tasks, Advance Verilog Topics- Timing and delays – types of delay models, path delay modeling, Timing checks, delay back-annotation, Switch level modeling – switch modeling elements, examples.	**10**	**CO2** **CO3** **CO3**
Unit IV Logic Synthesis with Verilog HDL- What is logic synthesis, impact of logic synthesis, Verilog hdl synthesis, synthesis design flow, RTL to gates (Example, Verification of gate level net list, modeling tips for logic synthesis, examples of sequential circuit synthesis.	**10**	**CO2**

References:

1. Verilog HDL - Samir Palnitkar (Pearson)
2. Verilog HDL Synthesis, A Practical Primer – J Bhasker
3. Digital Design: With an Introduction to Verilog HDL - M. Morris Mano
4. Design Through Verilog HDL - B.Bala Tripura Sundari T.R. Padmanabhan
5. FSM based HDL Design –Peter Minns, lan Elliott(Wiley)

Note for Examiner(s):

There are eight questions in all organized in four sections and each section is having two questions from each of the four units. The candidate shall have to attempt five questions in all, selecting at least one question from each unit.

Outcomes	**Internal Evaluation (40 Marks)**				**Semester End Examination (60 Marks)**
	Test1	**Test2**	**Test 3**	**Assignment(5)+Attendance(5)**	**SEE**
Marks	**15**	**15**	**15**	**10**	**60**
CO1	10	--	--	--	10
CO2	5	10	5	--	20
CO3	--	5	10	--	15
CO4	--	--	--	5	15

Course Code: MMVD 205	**Course Name:** Lab Work II	**L**	**T**	**P**	**C**
		0	**0**	**16**	**8**

Year and Semester	**1st Year** **2nd Semester**	**Contact hours per week:** (16 Hrs.) Exam: (4 Hrs.)	
Pre-requisite of course	**NIL**	**Evaluation**	
		Internal Assessment: 40	**Theory Examination: 60**

Course Objective:

1. To simulate the various processes involved in fabrication of MOS capacitor and its characteristics.
2. To do hands-on on the fabrication of MOS capacitor and its characterization.
3. To simulate different digital circuits using HDLs.
4. To simulate advanced level analog circuits using Cadence and PSpice.
5. To develop the skills of assembly language programming of 8051.
6. To do interfacing of 8051 with external circuits.

Course Outcomes:

CO1	Design synchronous and asynchronous digital circuits using Verilog HDL.
CO2	Design analog circuits using Tanner tools.
CO3	Design basic building blocks like sources, sinks, mirrors and Op-amp as well using Cadence tool.
CO4	Simulate various fabrication processes involved in MOS capacitor.
CO5	Apply the basic programming skills of Assembly Language in problem solving.

Mapping of Course Outcomes to Program Outcomes:

CO's	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3	3	2	2	2	3	2	2	2	3	1	3	3	3
CO2	3	3	2	3	2	3	2	2	2	3	1	3	3	3
CO3	3	3	2	3	2	2	3	2	3	2	1	3	3	3
CO4	3	3	2	2	3	2	3	2	3	2	1	3	3	3
CO5	3	3	2	2	3	3	3	2	2	2	1	3	3	3

List of experiment

1. Design and simulation of MOS capacitor using Process Simulation tool.
2. Fabrication and Characterization of MOS capacitor (I-V, C-V)
3. Write, simulate and demonstrate Verilog model code for various Digital circuits.

4. Advanced Analog Circuit simulation using Cadence and P-SPICE.
5. Data flow and arithmetic logical operations programs in assembly language.
6. “Interfacing of 8051 with external world” programs using assembly or embedded C

Course Code: MMVD 301 (Program Elective - I)	**Course Name:** Micro Electro Mechanical Systems (MEMS)	**L**	**T**	**P**	**C**
		4	**0**	**0**	**4**
Year and Semester	**2nd Year 3rdSemester**	**Contact hours per week:** (4 Hrs.) Exam: (3 Hrs.)			
Pre-requisite of course	**NIL**	**Evaluation**			
		Internal Assessment: 40	**Theory Examination: 60**		

Course Objective: -

1. To understand the need of MEMS Technology
2. To understand the basics, process, material and applications of MEMS.
3. Familiarization and understanding of design concepts and mechanics of selected devices.

Course Outcomes:

CO1	Understand characteristics, need and application of MEMS.
CO2	Understand Micromachining techniques for MEMS device fabrication.
CO3	Students will be able to Design and simulate MEMS devices using CAD tools.

Mapping of Course Outcomes to Program Outcomes:

CO's	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3	2	2	2	2	2	3	2	2	--	--	2	2	2
CO2	3	3	3	2	3	3	2	2	3	--	--	3	2	3
CO3	3	3	2	3	2	3	3	3	2	--	--	3	3	3

CONTENTS	**Hrs.**	**COs**
Unit I Overview of MEMS and Microsystems: Introduction Microsystem vs. MEMS, Microsystems and Microelectronics, the Multidisciplinary Nature of Microsystem design and manufacture, Application of MEMS in various industries. MEMS and Miniaturization: Scaling laws in miniaturization: Introduction to Scaling, Scaling in: Geometry, Rigid Body dynamics, Electrostatic forces, Electromagnetic forces, Electricity, Fluid Mechanics, Heat Transfer. Materials for MEMS and Microsystems – Si as substrate material, mechanical properties of Silicon, Silicon Compounds (SiO2, Si3N4, SiC, polySi, Silicon), Piezoresistors, GaAs, Piezoelectric crystals, Polymers, Packaging Materials.	**10**	**CO1**
Unit II Micromachining Processes: Overview of microelectronic fabrication processes used in MEMS, Bulk Micromachining – Isotropic & Anisotropic Etching, Comparison of Wet vs Dry etching, Surface Micromachining – General description, Processing in general, Mechanical Problems associated with Surface Micromachining, Introduction to LIGA process, and Introduction to Bonding. Assembly of 3D MEMS - foundry process	**10**	**CO2**

Unit III Microsystems & MEMS Design: Design Considerations: Design constraints, Selection of Materials, Selection of Manufacturing processes, Selection of Signal Transduction, Electromechanical system, packaging. Process design, Mechanical Design – Thermo mechanical loading, Thermo mechanical Stress Analysis, Dynamic Analysis, Interfacial fracture Analysis, Mechanical Design using Finite Element Method.	**10**	**CO3**
Unit IV Design case using CAD. Principles of Measuring Mechanical Quantities: Transduction from Deformation of Semiconductor Strain gauges: Piezo resistive effect in Single Crystal Silicon, Piezo resistive effect in Poly silicon Thin films, Transduction from deformation of Resistance. Capacitive Transduction: Electro mechanics, Diaphragm pressure sensors. Structure and Operation of Accelerometers, Resonant Sensors, Thermal Sensing and actuation.	**10**	**CO3**

References:

1. Microsystem Design By Stephen D. Senturia, Kluwer Academic Publishers (2003)
2. Micro Technology and MEMS By M. Elwenspoek and R. Wiegerink, Springer (2000)
3. Micro Fabrication by Marc Madaon, CRC Press
4. MEMS & Microsystems Design and Manufacture by Tai-Ran H Su, Tata Mc graw.

Note for Examiner(s):

There are eight questions in all organized in four sections and each section is having two questions from each of the four units. The candidate shall have to attempt five questions in all, selecting at least one question from each unit.

Assessment Pattern:

Outcomes	**Internal Evaluation (40 Marks)**				**Semester End Examination (60 Marks)**
	Test1	**Test2**	**Test 3**	**Assignment(5)+Attendance(5)**	**SEE**
Marks	**15**	**15**	**15**	**10**	**60**
CO1	15	--	--	--	25
CO2	--	15	--	--	20
CO3	--	--	15	5	15

Course Code: MMVD 301 (Program Elective II)	**Course Name:** RF Microelectronics	**L**	**T**	**P**	**C**
		4	**0**	**0**	**4**
Year and Semester	**2nd Year 3rd Semester**	**Contact hours per week:** (4 Hrs.) Exam: (3 Hrs.)			
Pre-requisite of course	**NIL**	**Evaluation**			
		Internal Assessment: 40	**Theory Examination: 60**		

Course Objective:

1. To understand RF technology, wireless technology and their application in IC design technology.
2. To perform RF network analysis.
3. To design noise optimization in RF circuits.
4. To design different RF microelectronics chips for various application.

Course Outcomes:

CO1	Understand the fundamentals of RF technology, wireless technology and their application in IC design technology
CO2	Apply the knowledge of RF Circuit and system in IC Design.
CO3	Analyze and design noise optimization in RF Circuits.
CO4	Design application based RF microelectronics Chip.

Mapping of Course Outcomes to Program Outcomes:

CO's	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3	2		3		1	3					2	2	2
CO2	3	2		3		2	2					2	3	3
CO3	3	2		2		3	2					3	3	3
CO4	3	2		2		3	2					3	2	2

CONTENTS	**Hrs.**	**COs**
Unit I Importance of RF and wireless technology, IC design technology for RF circuits RF Behavior of passive components, operation for passive components at RF Active RF Components, RF Diodes, RF BJTs, RF FET, HEMT Active RF component modeling, Transistor models.	**10**	**CO1**
Unit II Circuit representation of two port RF / Microwave Networks, Low and high frequency parameters, Formulation and properties of s parameters, Shifting reference plans, Transmission matrix, Generalized scattering parameters, Passive Circuit design, Review of Smith chart Matching and Biasing networks, Impedance matching using discrete components, micro strip line matching networks, amplifier classes of operation, RF Transistor amplifier designs, Low Noise amplifiers, Stability consideration, Constant gain noise figure circles.	**10**	**CO1 CO2**

Unit III Noise considerations in active networks, Noise definition, noise sources. RF / Microwave oscillator design, Oscillator versus amplifier design, Oscillation conditions, Design of transistor oscillators, Generator Tuning networks RF / Microwave Frequency conversion II: Mixer design, Mixer types, Conversion loss for SSB mixers, SSB mixer versus DSB mixers. One diode mixers, two diode mixers, Four diode mixers, eight diode mixers.	**10**	**CO3**
Unit IV Frequency synthesizers, PLL, RF synthesizer architectures, Transceiver architectures, Receiver architectures, Transmitter architectures, RF / Microwave IC design, Microwave ICs, MIC Materials, Types of MICs, Hybrid vs monolithic MICs, Case studies, Relating to design of different circuits employed in RF Microelectronics.	**10**	**CO4**

References

1. Behzad Razavi, "RF Microelectronics" Prentice Hall PTR , 1998
2. R.Ludwig, P.Bretchko, RF Circuit Design, Pearson Education Asia, 2000.
3. Matthew M. Radmanesh, Radio Frequency and Microwave Electronics Illustrated, Pearson Education (Asia) Ltd., 2001

Note for Examiner(s):

There are eight questions in all organized in four sections and each section is having two questions from each of the four units. The candidate shall have to attempt five questions in all, selecting at least one question from each unit.

Assessment Pattern:

Outcomes	**Internal Evaluation (40 Marks)**				**Semester End Examination (60 Marks)**
	Test1	**Test2**	**Test 3**	**Assignment(5)+Attendance(5)**	**SEE**
Marks	**15**	**15**	**15**	**10**	**60**
CO1	10	--	--	--	15
CO2	5	10	--	--	15
CO3	--	5	10	--	15
CO4	--	--	5	5	15

Course Code: MMVD 302 (Program Elective I)	**Course Name:** Embedded System Design using ARM	**L**	**T**	**P**	**C**
		4	**0**	**0**	**4**
Year and Semester	**2nd Year 3rd Semester**	**Contact hours per week:** (4 Hrs.) Exam: (3 Hrs.)			
Pre-requisite of course	**NIL**	**Evaluation**			
		Internal Assessment: 40	**Theory Examination: 60**		

Course Objective:

1. To understand the basics, architecture and programming of ARM processor.
2. To understand and explain the cache mechanism in ARM Processor.
3. To understand the Memory management Unit of ARM.

Course Outcomes:

CO1	Understand the fundamental concepts of ARM Processor, its architecture, instructions and modes as well.
CO2	Apply the basic programming skills in ARM with simple instructions.
CO3	Understand the Cache mechanism of ARM.
CO4	Understand the Memory management Unit of ARM.

Mapping of Course Outcomes to Program Outcomes:

CO's	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3			2		3	3	1	1			3	2	3
CO2	3			2		3	3	1	1			3	2	3
CO3	3			2		2	3	1	1			3	2	3
CO4	3			2		2	3	1	1			3	2	3

CONTENTS	**Hrs.**	**COs**
Unit I ARM PROCESSOR ARCHITECTURE: The RISC and ARM design philosophy, Embedded System Hardware. ARM PROCESSOR FUNDAMENTALS: Data Flow model, Registers, modes of operation, Current Program Status Register, Pipeline, Exceptions, Interrupts, and ARM families.	**10**	**CO1 CO2**
Unit II ARM INSTRUCTIONS SETS AND INTERRUPTS: ARM and Thumb Instruction Sets, Data Processing Instructions, Branch Instructions, Load- Store Instructions, Software Interrupt Instruction, Program Status Register Instructions, Conditional Execution, Stack Instructions, Software Interrupt Instruction. ARM PROCESSOR EXCEPTIONS AND MODES: vector table, priorities, link Register offsets, interrupts, and IRQ / FIQ exceptions interrupt stack design and implementation. SIMPLE PROGRAM: Addition, Subtraction, and Multiplication in assembly.	**10**	**CO2**

Unit III CACHE MECHANISM: Introduction to cache memory, memory hierarchy and cache memory, Cache architecture and cache policies. CONCEPT OF FLUSHING AND CLEANING CACHE: Flushing and Cleaning ARM cache core. CONCEPT OF CACHE LOCKDOWN: Locking Code and Data in Cache. Cache and write buffer.	**10**	**CO3**
Unit IV MEMORY MANAGEMENT UNIT: How virtual memory works, Details of the ARM MMU, Page Tables, Translation Look-aside Buffer, Domains and Memory access Permissions.	**10**	**CO4**

References:

1. "ARM System Developer's Guide Designing and Optimizing" by Andrew N.Sloss Elsevier publication, 2004.
2. "MicroC/OS – II" second edition The Real Time Kernel Jean J. Labrosse Publisher: Viva Books Private Ltd (Feb 2002)
3. "Embedded systems" B.Kanta Rao PHI publishers, Eastern Economy Edition, 2011
4. "Embedded Systems Architecture" - Tammy Noergard, Newness edition, 2005
5. "ARM System-on-Chip Architecture" 2nd Edition, Steve Furbe, Pearson Education, 2000
6. "Embedded/Real Time Systems" Dr. K.V.K.K PRASAD Dream tech press, 2009.

Note for Examiner(s):

There are eight questions in all organized in four sections and each section is having two questions from each of the four units. The candidate shall have to attempt five questions in all, selecting at least one question from each unit.

Assessment Pattern:

Outcomes	**Internal Evaluation (40 Marks)**				**Semester End Examination (60 Marks)**
	Test1	**Test2**	**Test 3**	**Assignment(5)+Attendance(5)**	**SEE**
Marks	**15**	**15**	**15**	**10**	**60**
CO1	10	--	--	--	15
CO2	5	10	--	5	15
CO3	--	5	10	--	15
CO4	--	--	5	--	15

Course Code: MMVD 302 (Program Elective II)	**Course Name:** Digital System Testing and Fault Simulation	**L**	**T**	**P**	**C**
		4	**0**	**0**	**4**
Year and Semester	**2nd Year 3rd Semester**	**Contact hours per week:** (4 Hrs.) Exam: (3 Hrs.)			
Pre-requisite of course	**NIL**	**Evaluation**			
		Internal Assessment: 40	**Theory Examination: 60**		

Course Objective:

1. To Understand basic concepts of digital system Testing
2. To understand the functional fault modeling at logic level as well as register level.
3. To describe various fault models like Functional Faults, Structural Faults, and Structural Gate Level Faults.
4. To understand various Automatic Test Generation algorithms for Single stuck Faults.
5. To explain simulations used for fault testing and various design for test-ability techniques.

Course Outcomes: On completion of the course, student would be able to:

CO1	To explain the Fundamental concepts of digital system testing.
CO2	Acquire knowledge about fault modeling and collapsing.
CO3	Analyze various ATPG Techniques for faults finding.
CO4	Develop fault simulation techniques and fault diagnosis methods.

Mapping of Course Outcomes to Program Outcomes:

CO's	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3	3		3		3	2	2	3	--	--	3	3	3
CO2	3	3		3		3	2	2	3	--	--	3	3	3
CO3	3	3		3		3	2	2	3	--	--	3	3	3
CO4	3	3		3		3	2	2	3	--	--	3	3	3

CONTENTS	**Hrs.**	**COs**
Unit I Role of testing in VLSI Design flow, Testing at different levels of abstraction. Functional Modeling at the logic Level, Functional Modeling at the Register Level, Structural Models, Level of Modeling. Types of Simulation, Compiled Simulation, Event-Driven Simulation, Delay Models. Basic of Test and role of HDLs in testing (Introduction only), Verilog HDL for Design and Test in combinational circuits and sequential circuits.	**10**	**CO1 CO2**
Unit II Fault Modeling:- Fault Abstraction, Functional Faults, Structural Faults, Structural Gate Level Faults, Recognizing Faults, Stuck-Open Faults, Stuck-at-0 Faults, Stuck-at-1 Faults, Bridging Faults, State-Dependent Faults, Multiple Faults, Single Stuck-at-Structural Faults, Detecting Single Stuck-at Fault, Detecting Bridging Faults, Fault Collapsing, Dominance Fault Collapsing, Fault Simulation:-Gate-Level Fault Simulation.	**10**	**CO2**

Unit III Testing for single step faults - Basic Issues, ATG algorithms for SSFs in Combinational Circuits: D, 9-V, PODEM Algorithms, Fault independent test generation, Sequential Circuit test generation.	**10**	**CO3** **CO4**
Unit IV Design for Test, Testing Sequential and Combinational Circuits, Ad Hoc Design for Testability Techniques, Testability insertion - Controllability and Observability concept, Full Scan Insertion, Flip - Flop Structures, General Aspects of Compression Techniques, Ones-Count Compression, LFSR used as signature analyzer , Introduction to BIST and MBIST.	**10**	**CO4**

References:

1. Digital systems testing and testable design – Miron Abramovici , Computer Science Press (1991).
2. Digital System Test and Testable Design: Using HDL Models and Architectures by Zainalabedin Navabi.
3. Test generation for VLSI chips by VD Agrawal and SC Seth, IEEE Computer Society Press (2003).
4. Essentials of Electronic Testing by ML Bushnell, VD Agrawal, Kluwer Academic Publishers.
5. VLSI Testing: digital and mixed analogue digital techniques Stanley L. Hurst Pub (1999).

Note for Examiner(s):

There are eight questions in all organized in four sections and each section is having two questions from each of the four units. The candidate shall have to attempt five questions in all, selecting at least one question from each unit.

Assessment Pattern:

Outcomes	**Internal Evaluation (40 Marks)**				**Semester End Examination (60 Marks)**
	Test1	**Test2**	**Test 3**	**Assignment(5)+Attendance(5)**	**SEE**
Marks	**15**	**15**	**15**	**10**	**60**
CO1	10	--	--	--	10
CO2	5	10	--	--	15
CO3	--	5	10	--	20
CO4	--	--	5	5	15

Course Code: MMVD 303 (Program Elective I)	**Course Name:** Nano Science and Technology		**L**	**T**	**P**	**C**
			4	**0**	**0**	**4**
Year and Semester	**2nd Year 3rdSemester**	**Contact hours per week:** (4 Hrs.) Exam: (3 Hrs.)				
Pre-requisite of course	**NIL**	**Evaluation**				
		Internal Assessment: 40	**Theory Examination: 60**			

Course Objectives:

1. Understand the fundamental forces controlling the dynamic and static response of materials at the Nano-scale
2. Demonstrate a comprehensive understanding of state-of-the-art of Nano-fabrication methods
3. Determine and evaluate the processing conditions to engineer functional nanomaterials
4. Design and analyze scalable system for the continuous production of nanomaterials
5. Practice and explain the state-of-the-art characterization methods for nanomaterials

Course Outcomes: On completion of the course, student would be able to:

CO1	Understand the Nanotechnology and Nano materials, bottom up and top down approaches of nanomaterials synthesis.
CO2	Understand the concept of Quantum devices: Resonant tunneling diode, Coulomb Blockade, Single Electron Transistor.
CO3	Understand the various Nano Material Synthesis techniques (ALD, MBE, CVD etc.)
CO4	Understand the growth mechanism, properties and devices applications of Carbon nanotubes.
CO5	Understand the Nano manipulation and Nano lithography: E-beam and Nano imprint lithography.
CO6	Understand the various Nano characterization techniques like : High Resolution TEM, Scanning Probe Microscopes: Atomic Force Microscope and Scanning Tunneling Microscope

Mapping of Course Outcomes to Program Outcomes:

CO's	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3	3	3	2	2	3	3	2	2	--	--	2	2	2
CO2	3	3	2	3	2	3	3	2	2	--	--	3	2	2
CO3	3	3	3	2	3	3	2	2	2	--	--	3	3	2
CO4	3	3	2	2	2	3	3	2	2	--	--	2	2	2
CO5	3	3	3	2	2	3	3	2	2	--	--	2	2	2
CO6	3	3	3	2	2	3	3	2	2	--	--	2	2	2

CONTENTS	Hrs.	COs
Unit I Introduction to Nanotechnology and Nano materials, History, ethical issues, applications in different fields, bottom up and top down approaches, Introduction to Zero, One and Two Dimensional Nanostructures, Quantum devices: Resonant tunneling diode, Coulomb Blockade, Single Electron Transistor.	**10**	**CO1** **CO2**
Unit II Nano Material Synthesis techniques Physical methods: ball milling, Atomic Layer Deposition, Molecular beam epitaxy , spray pyrolysis, Chemical Methods: Sol gel, self assembly, Chemical Vapor depositions, template manufacturing, biological synthesis	**10**	**CO3**
Unit III Carbon nanotubes, structures and synthesis, growth mechanism and properties, devices applications, Nanowires: synthesis and characterization, Molecular Switches and logic gates. Nano manipulation and nano lithography: E-beam and nano imprint lithography.	**10**	**CO4** **CO5**
Unit IV High resolution nano lithography, Dip-Pen lithography, AFM Lithography. Nano characterization: High Resolution TEM, Scanning Probe Microscopes: Atomic Force Microscope and Scanning Tunneling Microscope, Nano manipulator, Lab on a Chip concept	**10**	**CO6**

References:

1. Nanotechnology: Principle and Practices by Sulbha Kulkarni
2. Hand book of Nanotechnology By Bhushan , Springer
3. Nano: The Essentials By T. Pradeep
3. Microfabrication by Marc Madaon, CRC Press

Note for Examiner(s):

There are eight questions in all organized in four sections and each section is having two questions from each of the four units. The candidate shall have to attempt five questions in all, selecting at least one question from each unit.

Assessment Pattern:

Outcomes	Internal Evaluation (40 Marks)				Semester End Examination (60 Marks)
	Test1	Test2	Test 3	Assignment(5)+Attendance(5)	SEE
Marks	**15**	**15**	**15**	**10**	**60**
CO1	10	--	--	--	10
CO2	5	--	--	--	10
CO3	--	--	--	--	10
CO4	--	10	--	5	10
CO5	--	5	--	--	10
CO6	--	--	15	--	10

Course Code: MMVD 303 (Program Elective II)	**Course Name:** Digital Signal Processing in VLSI	**L**	**T**	**P**	**C**
		4	**0**	**0**	**4**
Year and Semester	**2nd Year 3rdSemester**	**Contact hours per week:** (4 Hrs.) Exam: (3 Hrs.)			
Pre-requisite of course	**NIL**	**Evaluation**			
		Internal Assessment: 40	**Theory Examination: 60**		

Course Objective:

1.	To explain the Characterization and classification of signals, applications and need of DSP in VLSI.
2.	To understand the concept of digital filters and FIR filters, their various types and comparison.
3.	To apply time domain representation of discrete time signals and systems.
4.	To understand various DSP algorithms used for VLSI applications.
5.	To relate the knowledge of DSP in the field of VLSI

Course Outcomes: On completion of the course, student would be able to:

CO1	Explain Characterization and classification of signals, applications and need of DSP in VLSI.
CO2	Understand the concept of digital filters and FIR filters, their various types and comparison.
CO3	Design efficient DSP algorithms used for VLSI applications.
CO4	Translate effective algorithm design to integrated circuit implementations.

Mapping of Course Outcomes to Program Outcomes:

CO's	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3	3		2	2	3	3	2	2			3	3	3
CO2	3	3		2	2	3	3	2	2			3	3	3
CO3	3	3		2	2	3	3	2	2			3	3	3
CO4	3	3		2	2	3	3	2	2			3	3	3

CONTENTS	**Hrs.**	**COs**
Unit I Introduction, Review of signals and signals processing, Enhancement of S/N, system models and the transfer function, spectra, limitations of Analog systems. Digital Signal Processing: Flexibility, key advantage to DSP, DSP issues and terminology, Sampled Data, Throughput expansion, data compression and pipelining. Non-recursive filters: Finite impulse response filters; Digital filters Recursive filters: Analog feedback filters and their recursive digital counterparts, Digital filter in block diagram form.	**10**	**CO1**
Unit II Digital Filter Overview: Digital filters, when, why, what, how? Comparison of digital filter types; summary of key digital filter relationships. FIR filters: FIR filter concepts and properties, Fourier-series approach to FIR filters; The window method of FIR filter design. FIR Filters: The second-order section as a prototype; Biquads for special purposes; Hardware implementation of FIR filters. The bridge to VLSI: Introduction, Some VLSI-DSP design Philosophy DSP, Architecture Issues: Tradeoffs, Pipelining, and parallelism.	**10**	**CO2**
Unit III Finite-word length arithmetic-Introduction, Arithmetic error sensitivity, Overflow, underflow, and rounding; filter quantization-error tradeoffs in fixed-point arithmetic, Accuracy in FFT		**CO3** **CO4**

spectral Analysis. Analog I/O methods Real DSP Hardware: Introduction, key, DSP hardware elements, System Selection: DSP system alternatives; Microcoded systems; Single-chip DSP microprocessor survey.	**10**	
Unit IV DSP applications: Introduction, Major elements of a DSP system, the digital Transceiver; Digital detection, Digital heterodyning, decimation and interpolation. Real-time detection: Examples based on correlation principles, coherent detection Modeling in Real time: Telecommunications and speech. Why modeling; Telecommunications; coding of speech. Image Processing: Introduction to image processing; Machine vision acquisition, enhancement, and recognition.	**10**	**CO4**

References:

1. Digital Signal Processing in VLSI by Richard J. Higgins (Prentice Hall)

Note for Examiner(s):

There are eight questions in all organized in four sections and each section is having two questions from each of the four units. The candidate shall have to attempt five questions in all, selecting at least one question from each unit.

Assessment Pattern:

Outcomes	**Internal Evaluation (40 Marks)**				**Semester End Examination (60 Marks)**
	Test1	**Test2**	**Test 3**	**Assignment(5)+Attendance(5)**	**SEE**
Marks	**15**	**15**	**15**	**10**	**60**
CO1	10	--	--	--	15
CO2	5	10	--	--	15
CO3	--	5	10	--	15
CO4	--	--	5	5	15

Course Code: MMVD 304	**Course Name:** Minor Project	**L**	**T**	**P**	**C**
		0	**0**	**16**	**8**
Year and Semester	**2nd Year 3rdSemester**	**Contact hours per week:** (16 Hrs.) Exam: (4 Hrs.)			
Pre-requisite of course	**NIL**	**Evaluation**			
		Internal Assessment: 0	**Theory Examination: 100**		

Course Objective:

1. To Study open ended research problem related to Microelectronics and VLSI design theoretical syllabus.
2. Present project findings and submit technical report.

Course Outcomes:

CO1	Identify the Topics that are relevant to the present context.
CO2	Identify the community that shall benefit through the solution to the identified engineering problem and also demonstrate concern for environment.
CO3	Analyze and interpret results of experiments conducted on the designed solution(s) to arrive at valid conclusions
CO4	Perform Survey and review relevant information.
CO5	Enhance Presentation skills and report writing skills.

Mapping of Course Outcomes to Program Outcomes:

CO's	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3	3	2	2	3	3	3	2	2	3	3	3	3	2
CO2	1	2	2	3		3		3	3		3	1	3	3
CO4	1	3		3		3	2	2	2		1	2	3	3
CO2	3	3	2	2	3	3	3	2	2	3	3	3	3	2
CO3	3	3	3	2	3	3	3	2	2	3	3	3	2	1

MMVD 401 - Project

Course Code: MMVD 401	**Course Name:** Project Dissertation		**L**	**T**	**P**	**C**
			0	**0**	**0**	**20**
Year and Semester	**2nd Year 4thSemester**	**Contact hours per week:** (-) Exam: (-)				
Pre-requisite of course	**NIL**	**Evaluation**				
		Internal Assessment: -	**Viva-Voce Examination: 300**			

Course Objective:

1.	To Study open ended research problem using appropriate techniques, tools and skills.
2.	Present project findings and submit technical papers and thesis.
3.	To learn about ways of literature survey in a given domain
4.	To understand the impact of scientific/industrial research/project on the society
5.	To know ways to carry out scientific research/ projects using existing scientific/technical knowledge
6.	To lean about financial management/planning of research project.
7.	To appreciate the importance of team work in professional environment
8.	To understand the professional ethics required in an industry/organization

Course Outcomes:

CO1	Conceptualize, design and implement solution for specific problem.
CO2	Communicate the solutions through presentation and technical report.
CO3	Apply project and resource management skills, Professional ethics and societal concerns.
CO4	Synthesize self-learning, sustainable solutions and demonstrate lifelong learning.

Mapping of Course Outcomes to Program Outcomes:

CO's	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**	**PSO3**
CO1	3	3	2	2	3	2	3	2	3	3	3	3	3	3
CO2	3	3	2	2	3	2	3	2	3	3	3	3	3	3
CO3	3	3	2	2	3	2	3	2	3	3	3	3	3	3
CO4	3	3	2	2	3	2	3	2	3	3	3	3	3	3