Kurukshetra University, Kurukshetra

(Established by the State Legislature Act-XII of 1956)
("A++" Grade, NAAC Accredited)

Syllabus of the Programme
for
Post Graduate Programme

M.Sc Electronic Science
I & II sem.

as per NEP 2020
Curriculum and Credit Framework for Postgraduate Programme

With Multiple Entry-Exit, Internship and CBCS-LOCF
With effect from the session 2024-25 (in phased manner)

DEPARTMENT OF ELECTRONIC SCIENCE
FACULTY OF SCIENCE

KURUKSHETRA UNIVERSITY, KURUKSHETRA -136119
HARYANA, INDIA

w.e.f. Session: 2024-25	
Part A - Introduction	
Name of Programme	M.Sc. Electronic Science
Semester	First
Name of the Course	Semiconductor Devices for Integrated Circuits
Course Code	M24-ELE-101
Course Type	CC1
Level of the course	400-499
Pre-requisite for the course	NIL
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO101.1: Describe the behavior of semiconductor materials and devices. CLO101.2: Reproduce the electrical characteristics of semiconductor junctions and use them in various semiconductor devices for switching and amplifications CLO101.3: Explain the behavior of Metal oxide semiconductor (MOS) systems with the help of energy band diagrams CLO101.4: Develop MOSFET devices with desired specifications for electronic circuit applications.

Credits	Theory	Practical	Total
	4	0	4
Teaching Hours per week	4	0	4
Internal Assessment Marks	30	0	30
End Term Exam Marks	70	0	70
Max. Marks	100	0	100
Examination Time	3 hours		

Part B- Contents of the Course

Instructions for Paper- Setter: The examiner will set 9 questions asking two questions from each unit and one compulsory question by taking course learning outcomes (CLOs) into consideration. The compulsory question (Question No. 1) will consist at least 4 parts covering entire syllabus. The examinee will be required to attempt 5 questions, selecting one question from each unit and the compulsory question. All questions will carry equal marks.

Unit	Topics	Contact Hours	CLOs
I	Band model in solids, donors and acceptors. Mass-Action law, effective mass. Carrier concentrations, Fermi level. Equilibrium Conditions-Electrons and holes. temperature dependence of carrier concentrations, compensation and space charge neutrality. Conductivity and mobility. Drift velocity and resistance. scattering, effect of temperature and doping on mobility, high field effect-velocity limitations. Hall effect Equilibrium in Electronic System. Idealized Metal-semiconductor junction. Current-voltage characteristics, non-rectifying contacts. Surface effects	15	CLO101.1
II	The pn junction, potential barrier, contact potential, equilibrium fermi levels. space charge at junction, forward and reverse biased junctions: Depletion width. electric field at junction, capacitance of pn junctions, (all concepts with suitable band diagrams) Reverse bias breakdown- Zener breakdown, avalanche breakdown Fundamentals of BJT operation, amplification with BJT's, BJT fabrication/structure (BJT for integrated circuits), terminal currents. Other important effects- drift in base region, base narrowing, avalanche breakdown, injection levels-thermal effects, Base resistance and emitter crowding, kirk effect.	15	CLO101.2

	Designing of amplifier circuits with BJT devices in common emitter configuration with (using emitter resistance) and without negative feedback		
III	Equilibrium in Electronic System, Idealized Metal-semiconductor junction, Current-voltage characteristics, non-rectifying contacts, Surface effects MOS structure, Ideal MOS capacitor, thermal equilibrium band diagrams, Polysilicon and metals as gate electrode materials, the flat band voltage, MOS Electronics -thermal equilibrium and nonequilibrium conditions, threshold voltage, Capacitance of MOS system- CV behaviour of Ideal MOS system, non-ideal MOS system- Effect of real surface, work function difference, Oxide and Interface charges, threshold voltage in presence of oxide charges	15	CLO101.3
IV	Basic MOSFET behaviour, Strong inversion region, current voltage characteristics, pinch off and saturation, Channel length modulation, body bias effect, Improved Models for short channel MOSFETs. Designing of MOSFET based amplifier circuits in common source configuration, Type of MOSFET Scaling – constant voltage and constant field scaling, short channel effects in MOSFET devices, Gate coupling, velocity overshoot, high field effects, substrate current, Hot carrier effects, Gate current, Device degradation, Structure that reduce the drain field.	15	CLO101.4
	Total Contact Hours	60	

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. Solid State Electronic Devices (6th edition) Ben G Streetman & S.K.Banerjee, (PHI, New Delhi, 2009)
2. Device Electronics for Integrated Circuits (3rd Edition) Muller & Kammins- John Wiley
3. Physics and Technology of Semiconductor Devices by A.S. Grove.
4. Physics of Semiconductor Devices by S.M.Sze.

Evaluation Method

Outcomes	Internal Assessment (30 Marks)			End Semester Examination (70 Marks)
	Mid Term Exam	Seminar/Presentation/ Assignment/Quiz/Test	Class Participation	SEE
Marks:	**15**	**10**	**5**	**70**
CLO101.1	7.5	-	-	17
CLO101.2	7.5		-	17
CLO101.3		5		18
CLO101.4		5		18

w.e.f. Session: 2024-25	
Part A – Introduction	
Name of Programme	M.Sc. Electronic Science
Semester	First
Name of the Course	IC Fabrication Technology
Course Code	M24-ELE-102
Course Type	CC2
Level of the course	400-499
Pre-requisite for the course	NIL
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO102.1: Describe various microelectronics fabrications technique/tools and instrumentation used for deposition of thin films. CLO102.2: Describe the kinetics of oxide layer growth on silicon surface and controlling the profile of dopants distribution in semiconductors. CLO102.3: Differentiate between various semiconductor processing techniques used for patterning (lithography and etching) of thin films and bulk structures. CLO102.4: Explain the process sequence for BJT, CMOS and BiCMOS Processes and their packaging.

Credits	Theory	Practical	Total
	4	0	4
Teaching Hours per week	4	0	4
Internal Assessment Marks	30	0	30
End Term Exam Marks	70	0	70
Max. Marks	100	0	100
Examination Time	3 hours		

Part B- Contents of the Course

Instructions for Paper- Setter: The examiner will set 9 questions asking two questions from each unit and one compulsory question by taking course learning outcomes (CLOs) into consideration. The compulsory question (Question No. 1) will consist at least 4 parts covering entire syllabus. The examinee will be required to attempt 5 questions, selecting one question from each unit and the compulsory question. All questions will carry equal marks.

Unit	Topics	Contact Hours	CLOs
I	Microelectronics processing: Introduction, Clean Room, Pure Water System, Vacuum Science and Technology, Practical vacuum systems, Operating principle: Rotary Pump, Cryo Pump and Turbo Molecular Pump, Vacuum Gauges: Pirani and Penning Gauge, Sources for vacuum deposition, Sputtering (DC, RF and RF Magnetron), Chemical Vapor Deposition, reactors for chemical vapor deposition, CVD Applications, PECVD, Metallization, Epitaxy: Introduction, Vapor phase epitaxy, Liquid phase epitaxy and Molecular beam epitaxy, Hetroepitaxy.	15	CLO102.1
II	Thermal Oxidation of Silicon, Oxide Formation, Kinetics of Oxide Growth, Oxidation Systems, Properties of Thermal Oxides of Silicon, Impurity Redistribution during Oxidation, Uses of Silicon Oxide, Basic diffusion process, Diffusion Equation, Diffusion Profiles, Evaluation of Diffused Layers, Diffusion in Silicon, Emitter-Push Effect, Lateral Diffusion, Distribution and Range of Implanted Ions, Ion Distribution, Ion Stopping, Ion Channeling, Disorder and Annealing, Multiple Implantation and Masking, Pre-	15	CLO102.2

	deposition and Threshold Control.		
III	Photolithography. Negative and Positive Photoresist. Resist Application. Exposure and Development. Photolithographic Process Control. E-Beam Lithography. X-Ray Beam Lithography and Ion Beam Lithography. Wet Chemical Etching. Chemical Etchants for SiO_2, Si_3N_4, Polycrystalline Silicon and other microelectronic materials. Plasma Etching. Plasma Etchants. Photoresist Removal. Lift off process. Etch Process Control	15	CLO102.3
IV	PMOS. NMOS and CMOS IC technology-fabrication steps with mask layout. MOS Memory technology- Static and Dynamic. Bipolar IC Technology. BiCMOS Technology. Packaging design considerations. Special package considerations. Yield loss in VLSI. Reliability requirements for VLSI.	15	CLO102.4
	Total Contact Hours	60	

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. Microelectronic Processing: An Introduction to the Manufacture of Integrated Circuits by W. Scot Ruska (McGraw Hill International Edition).
2. VLSI Technology by S. M. Sze (2nd Edition)
3. Microchip Fabrication: A Practical Guide to Semiconductor Processing by Peter Van Zant (2nd Edition) (McGraw Hill Publishing Company).
4. Vacuum Technology by A. Roth
5. Semiconductor Devices: Physics and Technology by S.M. Sze.
6. VLSI Fabrication Principles: Silicon and Gallium Arsenide by Sorab K. Ghandhi (John Wiley & Sons).

Evaluation Method

Outcomes	Internal Assessment (30 Marks)			End Semester Examination (70 Marks)
	Mid Term Exam	Seminar/Presentation/ Assignment/Quiz/Test	Class Participation	SEE
Marks :	**15**	**10**	**5**	**70**
CLO102.1	7.5	-	-	17
CLO102.2	7.5		-	17
CLO102.3		5		18
CLO102.4		5		18

w.e.f. Session: 2024-25			
Part A – Introduction			
Name of Programme	M.Sc. Electronic Science		
Semester	First		
Name of the Course	EM Theory and Electronic Communication		
Course Code	M24-ELE-103		
Course Type	CC3		
Level of the course	400-499		
Pre-requisite for the course	NIL		
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO103.1: Explain wave equation and boundary conditions CLO103.2: Understand the radio waves and analyze Smith chart for impedance matching CLO103.3: Explain various pulse and digital modulation techniques. CLO103.4: Understand the basics of modern telephone network and satellite communication		
Credits	Theory	Practical	Total
	4	0	4
Teaching Hours per week	4	0	4
Internal Assessment Marks	30	0	30
End Term Exam Marks	70	0	70
Max. Marks	100	0	100
Examination Time	3 hours		

Part B- Contents of the Course

Instructions for Paper- Setter: The examiner will set 9 questions asking two questions from each unit and one compulsory question by taking course learning outcomes (CLOs) into consideration. The compulsory question (Question No. 1) will consist at least 4 parts covering entire syllabus. The examinee will be required to attempt 5 questions, selecting one question from each unit and the compulsory question. All questions will carry equal marks.

Unit	Topics	Contact Hours	CLOs
I	Wave Equation and Boundary conditions, Plane monochromatic wave in non-conducting media, conducting media, Reflection and refraction at the boundary of two non-conducting media-oblique incidence, Reflection from a conducting plane-total internal reflection, Propagation between parallel conducting plates. Radio Wave propagation: Propagation in Free space, Tropospheric Propagation, Ionospheric propagation, Surface wave propagation, Propagation losses	15	CLO103.1
II	Transmission lines, Characteristic impedance, standing waves, quarter and half wavelength lines, Impedance matching, Use of Smith Chart, Impedance matching using Smith Chart, Losses in Transmission lines. Wave-guides: Rectangular, losses in Wave-guides, S Parameters, Basics of Antennas: Antenna parameters, Dipole antennas, Radiation pattern, Antenna gain.	15	CLO103.2
III	Pulse Communication, Pulse Amplitude modulation (PAM), Pulse Width Modulation, Pulse Position Modulation (PPM), Pulse Code Modulation and application. Digital Communication, Characteristics of Data Transmission Circuit, Data Transmission speeds, Noise, Cross talks, Echo suppressors, Distortion, Equalizers, Bit transmission, Signaling rate, Digital Communication techniques, FSK, PSK, BPSK, QPSK, DPSK, Error Detection and Correction codes.	15	CLO103.3
	Modern Telephone networks, mobile telephone network, intelligent network and		

IV	services (in brief). Satellite Communication: Introduction, Orbits, Station keeping, Satellite Attitude, Transmission Path, Path Loss, Noise considerations, the Satellite Systems, Saturation flux density, Effective Isotropic radiated Power, Multiple Access Methods.	15	CLO103.4
	Total Contact Hours	60	

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. Foundations of Electromagnetic Theory JR Reitz and FZ by Reitz and Milford (Addison Wesley).
2. Electromagnetics by B.B. Laud (Wiley Eastern).
3. Mathew N. O. Sadiku, 'Principles of Electromagnetics', 6th Edition, Oxford University Press Inc. Asian edition, 2015.
4. Theory and Applications of Microwaves by Brownwell and Beam (McGraw Hill).
5. Electronic Communication by George Kennedy.
6. Basic Electronic Communication by Roody & Coolen.
7. Electronic Communications System by Wayne Tomasi (Pearson).

Evaluation Method

Outcomes	Internal Assessment (30 Marks)			End Semester Examination (70 Marks)
	Mid Term Exam	Seminar/Presentation/ Assignment/Quiz/Test	Class Participation	SEE
Marks :	15	10	5	70
CLO103.1	7.5	-	-	17
CLO103.2	7.5		-	17
CLO103.3		5		18
CLO103.4		5		18

w.e.f. Session: 2024-25			
Part A - Introduction			
Name of Programme	M.Sc. Electronic Science		
Semester	First		
Name of the Course	Electronic Instrumentation and Control System		
Course Code	M24-ELE-104		
Course Type	CC4		
Level of the course	400-499		
Pre-requisite for the course	NIL		
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO104.1: Understand the characteristics of sensors and transducers and analyze their performance CLO104.2: Understand different methods for measuring a physical quantity and role of different instrumentation required for measuring the same CLO104.3: Identify different control systems, analyze using SFG and design these for specified purpose CLO104.4: Use different techniques to perform stability analysis of the designed control system and capability to do the state space analysis		
Credits	Theory	Practical	Total
	4	0	4
Teaching Hours per week	4	0	4
Internal Assessment Marks	30	0	30
End Term Exam Marks	70	0	70
Max. Marks	100	0	100
Examination Time	3 hours		

Part B- Contents of the Course

Instructions for Paper- Setter: The examiner will set 9 questions asking two questions from each unit and one compulsory question by taking course learning outcomes (CLOs) into consideration. The compulsory question (Question No. 1) will consist at least 4 parts covering entire syllabus. The examinee will be required to attempt 5 questions, selecting one question from each unit and the compulsory question. All questions will carry equal marks.

Unit	Topics	Contact Hours	CLOs
I	Basic concepts of measurement: Introduction, system configuration basic characteristics of measuring devices, Transducer Classification :Introduction, Electrical transducer, classification, basic requirements. Performance characteristics of an instrumentation system: generalized system, zero order, first order, second order system. Measurement of displacement: principle of transduction. Variable resistance device, LVDT, Variable capacitance transducer. Hall effect devices. Measurement of pressure: Thin film pressure transducer, piezoelectric pressure transducer vibrating element pressure transducer	15	CLO104.1 CLO104.2
II	Measurement of position, velocity, force, torque (basics only). Measurement of flow: Head type flow meters based on differential pressure measurements, Anemometers, Temperature measurements: resistance type temp. sensors, thermistors, thermocouples, solid state sensors, optical pyrometers, Measurement of humidity, thickness, pH (basics only). Instrumentation amplifier, Q meter, Digital storage oscilloscope, Lock-in Amplifier.	15	CLO104.2
	Bioelectrical signals and their measurement, Electrodes for ECG **Control System:** Introduction: Basic components of a control system, Example		

III	of control system applications, Open loop and closed loop control system, Feedback and its effects, Types of feedback control systems, Transfer functions, block diagram, and Signal Flow graphs. Time response of feedback control systems: Steady state error analysis, Introduction and design of P, I PI, PD and PID Controllers .	15	CLO104.3 CLO104.4
IV	Stability of linear control systems: introduction, Methods of determining stability, Routh –Hurwitz stability, Nyquist Stability Criterion, Root loci technique for analysis of LTI control system, Bode plots and Nyquist plots. **Introduction to State variable analysis:** Concepts of state, state variable and state models for electrical systems, Solution of state equations.	15	CLO104.3 CLO104.4
	Total Contact Hours	60	

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. Modern Electronic Instrumentation and Measurement Technique by Alfred D. Helfrick and William D. Cooper, (Eastern Economy Edition)
2. Instrumentation Devices and Systems by C.S. Rangan, G.R. Sarma and V.S.V Mani, Tata McGraw Hill.
3. Principles of Measurement and Instrumentation by Alan S. Morris, Prentice Hall.
4. Automatic Control Systems by Benjamin C. Kuo, Prentice Hall India.
5. Modern Control Engineering by K. Ogata, PHI.
6. Bio-Medical Instrumentation by R.S Khandpur.

Evaluation Method

Outcomes	Internal Assessment (30 Marks)			End Semester Examination (70 Marks)
	Mid Term Exam	Seminar/Presentation/ Assignment/Quiz/Test	Class Participation	SEE
Marks :	**15**	**10**	**5**	**70**
CLO104.1	7.5	-	-	17
CLO104.2	7.5		-	17
CLO104.3		5		18
CLO104.4		5		18

w.e.f. Session: 2024-25			
Part A - Introduction			
Name of the Programme	M.Sc Electronic Science		
Semester	First		
Name of the Course	Analog Circuits Design Lab		
Course Code	M24-ELE-105		
Course Type	PC1		
Level of the course	400-499		
Pre-requisite for the course	NIL		
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO105.1: Design analog electronics circuits based on semiconductor devices (Diode/BJT/MOSFET). CLO105.2: Implement application-oriented circuits using Op-amp &555 CLO105.3: Analyse & interpret the data obtained in the experiments CLO105.4: Present the experimental results and conclusions in the form of written report in clear and concise manner		
Credits	Theory	Practical	Total
	0	4	4
Teaching Hours per week	0	8	8
Internal Assessment Marks	0	30	30
End Term Exam Marks	0	70	70
Max. Marks	0	100	100
Examination Time	0	4 hours	

Part B- Contents of the Course

Practicals	**Contact Hours**
(List of experiments given here is tentative. it will be reviewed and updated at the beginning of every semester, as per the availability of expertise and equipment) **Tentative list of experiments** 1. Familiarization with electronic instruments like CRO, Multimeter, Function Generator etc. 2. Bipolar Junction Transistor based Amplifier Design (with & without Feedback) 3. Plot MOSFET characteristics and design common source amplifier. 4. Design of analog Multimeter 5. IC 555 applications: Monoshot, Astable, Bistable multivibrator, Schmitt Trigger etc, 6. OP- AMP based applications: Sample and hold circuits, logarithmic amplifier precision rectf. 7. OP- AMP Waver form generator, Triangular, Square & sine waver generators 8. Op- Based Active filters (IInd Order) – Low Pass, High Pass, Band Pass, Band Reject 9. Familiarization with Vaccum System and metal film deposition using thermal evaporation. 10. Wafer cleaning and verification of wafer type	120

Evaluation Method

Internal Assessment: 30		**End Term Examination: 70**	
➢ **Practicum**	**30**	➢ **Practicum**	**70**
• Class Participation:	5	Lab record, Viva-Voce, write-up and execution of the practical	
• Seminar/Demonstration/Viva-voce/Lab records etc.:	10		
• Mid-Term Exam:	15		

Part C-Learning Resources

Recommended Books/e-resources/LMS:

- Lab Manual of respective experiments

w.e.f. Session: 2024-25				
Part A - Introduction				
Name of the Programme	M.Sc Electronic Science			
Semester	First			
Name of the Course	Digital Circuit Design & Programming Lab			
Course Code	M24-ELE-106			
Course Type	PC2			
Level of the course	400-499			
Pre-requisite for the course (if any)	NIL			
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO106.1: Design combinational and sequential circuits using CMOS devices/ICs CLO106.2: Write a program/code using high level computer language for solving scientific problems CLO106.3: Analyse & interpret the data obtained in the experiments CLO106.4: Present the experimental results and conclusions in the form of written report in clear and concise manner			
Credits	Theory	Practical	Total	
	0	4	4	
Teaching Hours per week	0	8	8	
Internal Assessment Marks	0	30	30	
End Term Exam Marks	0	70	70	
Max. Marks	0	100	100	
Examination Time	0	4 hours		

Part B- Contents of the Course

Practicals	Contact Hours
(List of experiments given here is tentative. It will be reviewed and updated at the beginning of every semester as per the availability of expertise and equipment) **Tentative list of experiments** 1. Familiarization with Study of CMOS digital ICs families. 2. Design of digital inverter circuits using BJT devices and find out the noise margins from the transfer curve. 3. Design of synchronous and asynchronous digital counters. 4. Implementation of half adder and full adder circuit using CMOS digital ICS. 5. A/D and D/A converter circuits. 6. C-Programming- logical, arithmetic, decision making and loop operations. 7. C-Programming- file operations, functions & subroutines. 8. C-Programming- numerical methods 9. Plot device characteristics using C programs 10.Programming using MATLAB	120

Evaluation Method

Internal Assessment: 30		End Term Examination: 70	
➢ **Practicum**	**30**	➢ **Practicum**	**70**
• Class Participation:	5	Lab record, Viva-Voce, write-up and execution of the practical	
• Seminar/Demonstration/Viva-voce/Lab records etc.:	10		
• Mid-Term Exam:	15		

Part C-Learning Resources

Recommended Books/e-resources/LMS:

- Lab manuals of respective experiments

Chairman,
Electronic Science Deptt.
Kurukshetra University,
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w.e.f. Session: 2024-25	
Name of the Programme	M.Sc Electronic Science
Semester	First
Name of the Course	Seminar
Course Code	M24-ELE-107
Course Type: (CC/DEC/PC/Seminar/CHM/OEC/EEC)	Seminar
Level of the course	400-499
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO107.1: Establish motivation for any topic of interest in the field of electronics and analyze and data from literature survey. CLO107.2: Effective presentation and improve soft skills using new and recent technology for creating technical reports/presentation
Credits	Seminar
	2
Teaching Hours per week	2
Max. Marks	50
Internal Assessment Marks	0
End Term Exam Marks	50
Examination Time	1 hour

Instructions for Examiner: Evaluation of the seminar will be done by the internal examiner(s) on the parameters as decided by staff council of the department. There will be no external examination/viva-voce examination.

Chairman, Electronic ... Deptt. Kurukshetra ... sity, KURUKSHETRA ... 119.

w.e.f. Session: 2024-25			
Part A - Introduction			
Name of Programme	M.Sc. Electronic Science		
Semester	Second		
Name of the Course	Digital Circuits and System Design		
Course Code	M24-ELE-201		
Course Type	CC5		
Level of the course	400-499		
Pre-requisite for the course	NIL		
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO201.1: Understand and compare different CMOS logic families CLO201.2: Understand types of CMOS PLDs and implementation of basic circuits in VHDL CLO201.3: Analyze and design of State Machines CLO201.4: Define Impediments to Synchronous Design Methodology		
Credits	Theory	Practical	Total
	4	0	4
Teaching Hours per week	4	0	4
Internal Assessment Marks	30	0	30
End Term Exam Marks	70	0	70
Max. Marks	100	0	100
Examination Time	3 hours		

Part B- Contents of the Course

Instructions for Paper- Setter: The examiner will set 9 questions asking two questions from each unit and one compulsory question by taking course learning outcomes (CLOs) into consideration. The compulsory question (Question No. 1) will consist at least 4 parts covering entire syllabus. The examinee will be required to attempt 5 questions, selecting one question from each unit and the compulsory question. All questions will carry equal marks.

Unit	Topics	Contact Hours	CLOs
I	Introduction to CMOS Circuits, Logic families, CMOS logic, Electrical behaviour of CMOS circuits, CMOS steady state electrical behaviour, CMOS dynamic electrical behaviour, CMOS Input and Output structures, CMOS logic families, CMOS/TTL interfacing, Timing Hazards, Quine-McCluskey Method of finding Minimal SOP and POS Expressions.	14	CLO201.1
II	Combinational Logic Design Practice: Documentation standards, circuit timing, Combinational PLDs: Programmable logic array (PLA), Implementation of combinational logic using PLA, Programmable array logic (PAL), Generic Array logic (GAL), Description of some basic PLDs, Complex Programmable Logic Devices (CPLDs), Combinational PLD applications. Implementation of following in VHDL: decoders, encoders, three state devices, multiplexers, exclusive-OR gates and parity circuits, comparators, adders, combinational multipliers.	16	CLO201.2
III	Bistable elements, Latches and Flip-Flops, Clocked Synchronous State-machine Analysis, Clocked Synchronous State- machine Design, Designing State Machines using State Diagrams, State-machine Synthesis using Transition Lists.	15	CLO201.3
IV	Sequential PLDs, Registers: Shift Registers and counters, Iterative versus Sequential Circuits, Synchronous Design Methodology, Impediments to Synchronous Design, Synchronizer Failure and Meta stability, Field Programmable Gate Arrays.	15	CLO201.4
	Total Contact	60	

Hours	

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. Digital Design: Principles & Practices-John F. Wakerly (4th edition, Prentice Hall).
2. Programmable Logic: PLDs and FPGAs- R.C. Seals, G.F. Whapshott (McGraw-Hill, Publication)

Evaluation Method

Outcomes	Internal Assessment (30 Marks)			End Semester Examination (70 Marks)
	Mid Term Exam	Seminar/Presentation/ Assignment/Quiz/Test	Class Participation	SEE
Marks :	**15**	**10**	**5**	**70**
CLO201.1	7.5	-	-	17
CLO201.2	7.5		-	17
CLO201.3		5		18
CLO201.4		5		18

w.e.f. Session: 2024-25			
Part A - Introduction			
Name of Programme	M.Sc. Electronic Science		
Semester	Second		
Name of the Course	Analog CMOS Integrated Circuits		
Course Code	M24-ELE-202		
Course Type	CC6		
Level of the course	400-499		
Pre-requisite for the course	M24-ELE-101		
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO202.1: Describe the mathematical models for semiconductor devices and use it for circuit simulation. CLO202.2: Design various analog building blocks like switches, current mirrors and active resistors using MOSFET devices. CLO202.3: Analyze the performance of MOSFET based amplifier systems in integrated circuits. CLO202.4: Differentiate between various configurations of op-amp in terms of performance of Integrated Circuits.		
Credits	Theory	Practical	Total
	4	0	4
Teaching Hours per week	4	0	4
Internal Assessment Marks	30	0	30
End Term Exam Marks	70	0	70
Max. Marks	100	0	100
Examination Time	3 hours		

Part B- Contents of the Course

Instructions for Paper- Setter: The examiner will set 9 questions asking two questions from each unit and one compulsory question by taking course learning outcomes (CLOs) into consideration. The compulsory question (Question No. 1) will consist at least 4 parts covering entire syllabus. The examinee will be required to attempt 5 questions, selecting one question from each unit and the compulsory question. All questions will carry equal marks.

Unit	Topics	Contact Hours	CLOs
I	Device Modeling, DC models, small signal models, use of device models in circuit analysis, diode models, dc diode model, small signal diode model, HF diode model, MOS models, large signal (or dc) MOSFET model, small signal MOSFET model, HF MOSFET model, short channel Devices, sub-threshold MOS Models, Modeling noise sources in MOSFET's. MOS Device Layouts, Circuit simulation, Circuit simulation using SPICE, MOS SPICE Models.	14	CLO202.1
II	MOS switches, MOS Diode/active resistors, Current sources and sinks, Basic Current Mirrors, Cascoded Current Mirror, Widlar & Wilson Current mirror CMOS amplifiers: Single stage MOS Inverting Amplifier with various load configurations (resistive, diode connected, and current source as load), CMOS Push Pull amplifier	15	CLO202.2
III	Differential amplifiers: Qualitative and quantitative analysis, CMOS differential amplifiers -Differential pair with active loads, Differential pair with current source and current mirror load, Frequency response of Amplifiers: Concept of zeros and poles, Miller effect, Association of poles with nodes, frequency response of MOS inverting amplifiers and differential amplifiers.	16	CLO202.3

IV	CMOS two stage OP Amp, Stability and frequency compensation, Multipole system, Concept of phase margin, frequency compensation, compensation of two stage op-amp Simulation and measurement of op-amps, Comparators, characterization of comparators, High gain comparators, Propagation delay of two-stage comparators, Comparators using positive feedback, Autozeroing.	15	CLO202.4
	Total Contact Hours	60	

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. Design of analog CMOS Integrated Circuits, Behzad Razavi, Tata McGraw Hill
2. VLSI Design Techniques for Analogue and Digital Circuits by R.L. Geiger, P.E. Allen and N.R. Strader.
3. Analysis and Design of Analogue I.C's (2nd edition) by P.R. Gray, R.G. Meyer.
4. The SPICE book by Andrei Vladimirescu.
5. Computer Simulation of Electronic Circuits by Raghuram.

Evaluation Method

Outcomes	Internal Assessment (30 Marks)			End Semester Examination (70 Marks)
	Mid Term Exam	Seminar/Presentation/ Assignment/Quiz/Test	Class Participation	SEE
Marks :	**15**	**10**	**5**	**70**
CLO202.1	7.5	-	-	17
CLO202.2	7.5		-	17
CLO202.3		5		18
CLO202.4		5		18

w.e.f. Session: 2024-25			
Part A - Introduction			
Name of Programme	M.Sc. Electronic Science		
Semester	Second		
Name of the Course	Verilog Hardware Description Language		
Course Code	M24-ELE-203		
Course Type	CC7		
Level of the course	400-499		
Pre-requisite for the course	NIL		
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO203.1: Understand the basics of Verilog Hardware Description Language CLO203.2: Design Verilog models for digital circuits using Gate level, Dataflow and Switch level modelling CLO203.3: Design Verilog models for digital circuits using behavioural level modelling, and using Generate blocks, tasks and functions CLO203.4: Use delays, UDPs and the concept of synthesis and verification in Verilog models		
Credits	Theory	Practical	Total
	4	0	4
Teaching Hours per week	4	0	4
Internal Assessment Marks	30	0	30
End Term Exam Marks	70	0	70
Max. Marks	100	0	100
Examination Time	3 hours		

Part B- Contents of the Course

Instructions for Paper- Setter: The examiner will set 9 questions asking two questions from each unit and one compulsory question by taking course learning outcomes (CLOs) into consideration. The compulsory question (Question No. 1) will consist at least 4 parts covering entire syllabus. The examinee will be required to attempt 5 questions, selecting one question from each unit and the compulsory question. All questions will carry equal marks.

Unit	Topics	Contact Hours	CLOs
I	Benefits of CAD, Integrated circuit design techniques, Hierarchical design, Design abstraction, Computer aided design, Concepts of CPLD, FPGA. Introduction to HDLs, Verilog and its capabilities, Hierarchical Modeling Concepts: Design Methodologies, Modules, Instances, Components of Simulation and Test Bench. Basic Concepts: Lexical Conventions, Data Types, System Tasks and Compiler Directives, Modules and Ports.	15	CLO203.1
II	Gate-Level Modeling: Gate Types, Gate Delays, Dataflow Modeling, Continuous Assignments, Delays, Expressions, Operators, and Operands, Operator Types, Switch-Level Modeling: Switch-Modeling Elements.	15	CLO203.2
III	Behavioral Modeling: Structured Procedures, Procedural Assignments, Timing Controls, Conditional Statements, Multiway Branching, Loops, Sequential and Parallel Blocks, Generate Blocks, Tasks and Functions.	15	CLO203.3
IV	Timing and Delays, Types of Delay Models, Path Delay Modeling, Timing Checks, Delay Back-Annotation, User-Defined Primitives (brief), Programming Language Interface (brief), Logic Synthesis with Verilog, Synthesis Design Flow, Verification of Gate-Level Netlist, Verification Techniques (brief) :	15	CLO203.4

	Traditional Verification Flow, Assertion Checking, Formal Verification		
	Total Contact Hours	60	

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. Custom VLSI Microelectronics by Stanley L.Hurst (Prentice Hall 1992)
2. Verilog HDL - Samir Palnitkar (Pearson)
3. A Verilog HDl Primer - J. Bhaskar (Pearson)
4. Modern VLSI Design- A Systems Approach- Wayne Wolf-PTR Prentice Hall-1994

Evaluation Method

Outcomes	Internal Assessment (30 Marks)			End Semester Examination (70 Marks)
	Mid Term Exam	Seminar/Presentation/ Assignment/Quiz/Test	Class Participation	SEE
Marks :	**15**	**10**	**5**	**70**
CLO203.1	7.5	-	-	17
CLO203.2	7.5		-	17
CLO203.3		5		18
CLO203.4		5		18

w.e.f. Session: 2024-25			
Part A - Introduction			
Name of Programme	M.Sc. Electronic Science		
Semester	Second		
Name of the Course	Introduction to Embedded Systems		
Course Code	M24-ELE-204		
Course Type	CC8		
Level of the course	400-499		
Pre-requisite for the course	NIL		
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO204.1: Understand need and applications of the Embedded Systems CLO204.2: Analyse given problem and write programs using 8051 assembly language CLO204.3: Design interfacing circuits using standard peripherals CLO204.4: Understand the issues with hardware-software co-design		
Credits	Theory	Practical	Total
	4	0	4
Teaching Hours per week	4	0	4
Internal Assessment Marks	30	0	30
End Term Exam Marks	70	0	70
Max. Marks	100	0	100
Examination Time	3 hours		

Part B- Contents of the Course

Instructions for Paper- Setter: The examiner will set 9 questions asking two questions from each unit and one compulsory question by taking course learning outcomes (CLOs) into consideration. The compulsory question (Question No. 1) will consist at least 4 parts covering entire syllabus. The examinee will be required to attempt 5 questions, selecting one question from each unit and the compulsory question. All questions will carry equal marks.

Unit	Topics	Contact Hours	CLOs
I	**Introduction to Embedded Systems** : what is an Embedded system? , Embedded Systems vs General Computing Systems, Classification, major application areas, purpose of Embedded Systems, Wearable devices as an example of Embedded Systems **The Typical Embedded system** : Core of Embedded System, Memory, Sensors and Actuators, Communication Interface, Embedded Firmware, other system components	15	CLO204.1
II	Characteristics and Quality Attributes of Embedded Systems, Washing machine as application specific Embedded System and Automotive as domain specific embedded system **Designing Embedded Systems with 8bit Microcontrollers-8051:** controller selection, why 8051? **Designing with 8051 Microcontroller :** 8051 architecture, Memory Organization, Oscillator Unit, Ports, Interrupts, Timer Units, Serial Port, Reset Circuitry, Power saving modes	15	CLO204.2
III	**Programming the 8051 Microcontroller :** Addressing modes , Instruction Set – Data transfer, Arithmetic,Logical Instructions, Boolean Instructions, Program Control Transfer Instructions, **ALP for implementation of Instruction set** :binary to unpacked BCD, data transfer to internal and external memory, delay using timers **Design Examples** :number display on LED, 7-segment display, stepper motor control, Analog to Digital Converter Interfacing, serial data transmission.	16	CLO204.3
	Hardware-Software Co-Design and Program Modelling : Issues in Hardware-		

IV	Software Co-Design, Computational Models in Embedded Systems, Introduction to Unified Modelling Language.	14	CLO204.4
	Total Contact Hours	60	

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. Introduction to Embedded Systems : Shibu K. V. (TMH)
2. Embedded Systems: Architecture, Programming and Design ,2nd Edition, Raj Kamal, Tata-McGraw Hill, 2011.
3. The 8051 Microcontroller and Embedded Systems Using Assembly and C Second Edition, Muhammad Ali Mazidi, Janice Gillispie Mazidi, Rolin D. McKinlay, Pearson.
4. Advanced Microprocessors and Peripherals, 3rd Edition, Ray and Bhurchandi, Tata McGraw Hill, 2006.
5. The 8051 Micro controller 3rd Edition, Keneth Ayala, Cengage Publishers.

Evaluation Method

Outcomes	Internal Assessment (30 Marks)			End Semester Examination (70 Marks)
	Mid Term Exam	Seminar/Presentation/ Assignment/Quiz/Test	Class Participation	SEE
Marks :	**15**	**10**	**5**	**70**
CLO204.1	7.5	-	-	17
CLO204.2	7.5		-	17
CLO204.3		5		18
CLO204.4		5		18

w.e.f. Session: 2024-25			
Part A - Introduction			
Name of the Programme	M.Sc Electronic Science		
Semester	Second		
Name of the Course	Electronic Circuit Simulation and Embedded Systems Lab		
Course Code	M24-ELE-205		
Course Type	PC3		
Level of the course	400-499		
Pre-requisite for the course	NIL		
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO205.1: Perform the simulation of analog electronic circuits involving BJT/MOSFET Devices using LTSPICE and Cadence Tools CLO205.2: Be proficient in use of IDE's for designing, testing of microcontroller-based system CLO205.3: Analyze & interpret the data obtained in the experiments CLO205.4: Present the experimental results and conclusions in the form of written report in clear and concise manner		
Credits	Theory	Practical	Total
	0	4	4
Teaching Hours per week	0	8	8
Internal Assessment Marks	0	30	30
End Term Exam Marks	0	70	70
Max. Marks	0	100	100
Examination Time	0	4 hours	

Part B- Contents of the Course

Practicals	**Contact Hours**
(List of experiments given here is tentative. It will be reviewed and updated, at the beginning of every semester as per the availability of expertise and equipment) **Tentative list of experiments** 1. CMOS inverting Amplifier Circuits simulation using EDA Tools (Cadence Tools) 2. CMOS Differential Amplifiers with Active Loads using EDA Tools 3. Design and simulation of MOS Current sources 4. Design and Simulation of Current Mirror Circuits (Cascoded/Widler/Wilson) 5. Design and Simulation of first and second order Active Filter Circuits. 6. TCAD Simulation of semiconductor devices and processes. 7. Simulation of MEMS structures 8. Programming of 8051 using data flow instructions 9. Programming of 8051 using jump instructions 10. Use of external memories using 8051	120

Evaluation Method

Internal Assessment: 30		**End Term Examination: 70**	
➢ **Practicum**	**30**	➢ **Practicum**	**70**
• Class Participation:	5	Lab record, Viva-Voce, write-up and execution of the practical	
• Seminar/Demonstration/Viva-voce/Lab records etc.:	10		
• Mid-Term Exam:	15		

Part C-Learning Resources

Recommended Books/e-resources/LMS:

- Lab Manuals of the respective experiments

w.e.f. Session: 2024-25			
Part A - Introduction			
Name of the Programme	M.Sc Electronic Science		
Semester	Second		
Name of the Course	IC fabrication and characterization Lab		
Course Code	M24-ELE-206		
Course Type	PC4		
Level of the course	400-499		
Pre-requisite for the course (if any)	M24-ELE102		
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO206.1: Measure the parameters of semiconductor materials and device. CLO206.2: To use the techniques and equipment used for fabrication of semiconductor devices and integrated circuits. CLO206.3: To Analyze and interpret experimental data CLO206.4: Present the experimental results and conclusions in the form of written report in clear and concise manner		
Credits	Theory	Practical	Total
	0	4	4
Teaching Hours per week	0	8	8
Internal Assessment Marks	0	30	30
End Term Exam Marks	0	70	70
Max. Marks	0	100	100
Examination Time	0	4 hours	

Part B- Contents of the Course

Practicals	Contact Hours
(List of experiments given here is tentative. It will be reviewed and updated at the beginning of every semester as per the availability of expertise and equipment) **Tentative list of experiments** 1. Study of Hall Effect 2. Resistivity measurement using four probe setup 3. Study of PN junction parameters 4. Study of optoelectronic devices and solar cell 5. Characteristics of semiconductor power devices: UJT and SCR 6. Oxidation of silicon wafers (both wet & Dry) and oxide thickness measurement 7. Pattern transfer using photolithography (using positive photoresist) 8. Wet etching of oxide and Aluminum film 9. Metal-Semiconductor Contact Fabrication & characterization 10. MOS Fabrication & its CV Characterization	120

Evaluation Method

Internal Assessment: 30		End Term Examination: 70	
➢ **Practicum**	**30**	**Practicum**	**70**
• Class Participation:	5	Lab record, Viva-Voce, write-up and execution of the practical	
• Seminar/Demonstration/Viva-voce/Lab records etc.:	10		
• Mid-Term Exam:	15		

Part C-Learning Resources

Recommended Books/e-resources/LMS:

- Lab Manuals of the respective experiments