KURUKSHETRA UNIVERSITY KURUKSHETRA

Scheme of Examination and Syllabus

for

Under-Graduate Programme

Subject: Electronic Equipment & Maintenance

7th & 8th Semester

Under Multiple Entry-Exit, Internship and CBCS-LOCF in accordance to NEP-2020 w.e.f. 2025-26

Revised Scheme of Examination for Under-Graduate Programme
Under Multiple entry-Exit, Internship and CBCS-LOCF in accordance to NEP-2020
w.e.f. 2025-26. Subject: Electronic Equipment & Maintenance

FOURTH YEAR: SEMESTER-7 (FOR HONOURS/HONOURS WITH RESEARCH IN ELECTRONIC EQUIPMENT & MAINTENANCE)

Remarks	Course	Paper(s)	Nomenclature of Paper	Credits	Hours/ Week	Internal marks	External Marks	Total Marks	Exam Duration
for Honours in Electronics/ Honours with Research in Electronic Equipment & Maintenance (For Scheme B & C)	CC-H1 4 credit	B23-EEM-701	Solid State Electronic Devices	4	4	30	70	100	3 hrs.
	CC-H2 4 credit	B23-EEM-702	Microelectronics Processing & Technology	4	4	30	70	100	3 hrs.
	CC-H3 4 credit	B23-EEM-703	Electronic Communication-3	4	4	30	70	100	3 hrs.
	DSE-H1 4 credit Select one Option	B23-EEM-704	Instrumentation & Control System	4	4	30	70	100	3 hrs.
		B23-EEM-705	CAD Tools for Microelectronics	4	4	30	70	100	3 hrs.
	PC-H1 4 credit	B23-EEM-706	Practical Based on B23-EEM-701 TO 704/705	4	8	30	70	100	6 hrs.
	CC-HM1 4 credit	From Available Minor of 4 credits as per NEP							

SEMESTER-8 (FOR HONOURS IN ELECTRONIC EQUIPMENT & MAINTENANCE)

Remarks	Course	Paper(s)	Nomenclature of Paper	Credits	Hours/ Week	Internal marks	External Marks	Total Marks	Exam Duration
Honours in Electronic Equipment & Maintenance (For Scheme B & C)	CC-H4 4 credit	B23-EEM-801	CMOS and PLD Logic Design	4	4	30	70	100	3 hrs.
	CC-H5 4 credit	B23-EEM-802	MOS Device Modeling and CMOS Amplifier Design	4	4	30	70	100	3 hrs.
	CC-H6 4 credit	B23-EEM-803	Verilog Hardware Description Language	4	4	30	70	100	3 hrs.
	DSE-H2 4 credit Select one option	B23-EEM-804	Embedded Systems Design	4	4	30	70	100	3 hrs.
		B23-EEM-805	Advanced Digital Communication Systems	4	4	30	70	100	3 hrs.
	PC-H2 4 credit	B23-EEM-806	Practical Based on B23-EEM-801 TO 804/805	4	8	30	70	100	6 hrs.
	CC-HM2 4 credit	From Available Minor of 4 credits as per NEP							

OR SEMESTER-8 (FOR HONOURS WITH RESEARCH IN ELECTRONIC EQUIPMENT & MAINTENANCE)

Remarks	Course	Paper(s)	Nomenclature of Paper	Credits	Hours/ Week	Internal marks	External Marks	Total Marks	Exam Duration
Honours with Research in Electronic Equipment & Maintenance (For Scheme B & C)	CC-H4 4 credit	B23-EEM-801	CMOS and PLD Logic Design	4	4	30	70	100	3 hrs.
	CC-H5 4 credit	B23-EEM-802	MOS Device Modeling and CMOS Amplifier Design	4	4	30	70	100	3 hrs.
	Project/Dissertation 12 credit	B23-EEM-807	Project/Dissertation	8+4	-	-	300	300	-
	CC-HM2 4 credit	From Available Minor of 4 credits as per NEP							

Session:2025-26			
Part A - Introduction			
Subject	ELECTRONIC EQUIPMENT MAINTENANCE		
Semester	SEVENTH		
Name of the Course	Solid State Electronic Devices		
Course Code	B23-EEM-701		
Course Type: (CC/MCC/MDC/CC-M/DSEC/VOC/DSE/PC/AEC/VAC)	CC-H1		
Level of the course	400-499		
Pre-requisite for the course (if any)	Basic knowledge of Semiconductor Physics		
Course Learning Outcomes (CLO):	After completing this course, the learner will be able to: 1. Describe the behaviour of semiconductor materials and devices. 2. Reproduce the electrical characteristics of semiconductor Junctions and use them in various semiconductor devices for switching and amplifications 3. Explain the behaviour of Metal oxide semiconductor (MOS) systems with the help of energy band diagrams 4. Develop MOSFET devices with desired specifications for electronic circuit applications.		
Credits	Theory	Practical	Total
	4	-	4
Contact Hours	60	-	60
Max. Marks: 100 Internal Assessment Marks: 20 Theory End Term Exam Marks:80Theory		Exam Time: 3 Hours	

Part B - Contents of the Course

Instructions for Paper-Setter

1. Nine questions will be set in all. All questions will carry equal marks.
2. Question No.1, which will be short answer type covering the entire syllabus, will be compulsory. The remaining eight questions will be set unit wise selecting two questions from each Unit I to IV. The candidate will be required to attempt question No. 1 and four more questions selecting one question from each unit

Unit	Topics	Contact Hours
I	Band model in solids, donors and acceptors, Mass-Action law, effective mass, Carrier concentrations, Fermi level, Equilibrium Conditions-Electrons and holes, temperature dependence of carrier concentrations, compensation and space charge neutrality, Conductivity and mobility, Drift velocity and resistance, scattering, effect of temperature and doping on mobility, high field effect-velocity limitations, Hall effect Equilibrium in Electronic System, Idealized Metal-semiconductor junction, Current-voltage characteristics, non-rectifying contacts, Surface effects	15
II	The pn junction, potential barrier, contact potential, equilibrium fermi levels, space charge at junction, forward and reverse biased junctions; Depletion width, electric field at junction, capacitance of pn junctions, (all concepts with suitable band diagrams) Reverse bias breakdown-Zener breakdown, avalanche breakdown Fundamentals of BJT operation, amplification with BJT's, BJT fabrication/structure (BJT for integrated circuits), terminal currents,	15

	Other important effects- drift in base region, base narrowing, avalanche breakdown, injection levels-thermal effects, Base resistance and emitter crowding, kirk effect, Designing of amplifier circuits with BJT devices in common emitter configuration with (using emitter resistance) and without negative feedback	
III	Equilibrium in Electronic System, Idealized Metal-semiconductor junction, Current-voltage characteristics, non-rectifying contacts, Surface effects MOS structure, Ideal MOS capacitor, thermal equilibrium band diagrams, Polysilicon and metals as gate electrode materials, the flat band voltage, MOS Electronics -thermal equilibrium and nonequilibrium conditions, threshold voltage, Capacitance of MOS system- CV behaviour of Ideal MOS system, non-ideal MOS system- Effect of real surface, work function difference, Oxide and Interface charges, threshold voltage in presence of oxide charges	15
IV	Basic MOSFET behaviour, Strong inversion region, current voltage characteristics, pinch off and saturation, Channel length modulation, body bias effect, Improved Models for short channel MOSFETs. Designing of MOSFET based amplifier circuits in common source configuration. Type of MOSFET Scaling – constant voltage and constant field scaling, short channel effects in MOSFET devices, Gate coupling, velocity overshoot, high field effects, substrate current, Hot carrier effects, Gate current, Device degradation, Structure that reduce the drain field.	15

Suggested Evaluation Methods

Internal Assessment:

➢ **Theory 30 Marks**

- Class Participation: **5 Marks**
- Seminar/presentation/assignment/quiz/class test etc.:**10 Marks**
- Mid-Term Exam: **15 Marks**

End Term Examination: 70 Marks

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. Solid State Electronic Devices (6th edition) Ben G Streetman & S.K.Banerjee, (PHI, New Delhi, 2009)
2. Device Electronics for Integrated Circuits (3rd Edition) Muller & Kammins- John Wiley
3. Physics and Technology of Semiconductor Devices by A.S. Grove.
4. Physics of Semiconductor Devices by S.M.Sze.

Session:2025-26			
Part A - Introduction			
Subject	ELECTRONIC EQUIPMENT MAINTENANCE		
Semester	SEVENTH		
Name of the Course	Microelectronics Processing & Technology		
Course Code	B23-EEM-702		
Course Type: (CC/MCC/MDC/CC-M/DSEC/VOC/DSE/PC/AEC/VAC)	CC-H2		
Level of the course	400-499		
Pre-requisite for the course(if any)	Basic knowledge of Semiconductor Physics		
Course Learning Outcomes (CLO):	After completing this course, the learner will be able to: 1. Describe various microelectronics fabrications technique/tools and instrumentation used for deposition of thin films. 2. Describe the kinetics of oxide layer growth on silicon surface and controlling the profile of dopants distribution in semiconductors. 3. Differentiate between various semiconductor processing techniques used for patterning (lithography and etching) of thin films and bulk structures. 4. Explain the process sequence for BJT, CMOS and BiCMOS Processes and their packaging.		
Credits	**Theory**	**Practical**	**Total**
	4	-	4
Contact Hours	60	-	60
Max. Marks: 100 Internal Assessment Marks: 30 End Term Exam Marks:70		Exam Time: 3 Hours	

Part B-Contents of the Course

Instructions for Paper-Setter

1. Nine questions will be set in all. All questions will carry equal marks.
2. Question No.1, which will be short answer type covering the entire syllabus, will be compulsory. The remaining eight questions will be set unit wise selecting two questions from each Unit I to IV. The candidate will be required to attempt question No. 1 and four more questions selecting one question from each unit

Unit	Topics	Contact Hours
I	Microelectronics processing: Introduction, Clean Room, Pure Water System, Vacuum Science and Technology, Practical vacuum systems, Operating principle: Rotary Pump, Cryo Pump and Turbo Molecular Pump, Vacuum Gauges: Pirani and Penning Gauge, Sources for vacuum deposition, Sputtering (DC, RF and RF Magnetron), Chemical Vapor Deposition, reactors for chemical vapor deposition, CVD Applications, PECVD, Metallization, Epitaxy: Introduction, Vapor phase epitaxy, Liquid phase epitaxy and Molecular beam epitaxy, Hetroepitaxy.	**15**
II	Thermal Oxidation of Silicon, Oxide Formation, Kinetics of Oxide Growth, Oxidation Systems, Properties of Thermal Oxides of Silicon, Impurity Redistribution during Oxidation, Uses of Silicon Oxide, Basic diffusion process, Diffusion Equation, Diffusion Profiles, Evaluation of Diffused	**15**

	Layers, Diffusion in Silicon, Emitter-Push Effect, Lateral Diffusion, Distribution and Range of Implanted Ions, Ion Distribution, Ion Stopping, Ion Channeling, Disorder and Annealing, Multiple Implantation and Masking, Pre-deposition and Threshold Control.	
III	Photolithography, Negative and Positive Photoresist, Resist Application, Exposure and Development, Photolithographic Process Control. E-Beam Lithography, X-Ray Beam Lithography and Ion Beam Lithography. Wet Chemical Etching, Chemical Etchants for SiO_2, Si_3N_4, Polycrystalline Silicon and other microelectronic materials, Plasma Etching, Plasma Etchants, Photoresist Removal, Lift off process, Etch Process Control	**15**
IV	PMOS, NMOS and CMOS IC technology-fabrication steps with mask layout, MOS Memory technology- Static and Dynamic, Bipolar IC Technology, BiCMOS Technology, Packaging design considerations, Special package considerations, Yield loss in VLSI, Reliability requirements for VLSI.	**15**

Suggested Evaluation Methods

Internal Assessment: ➢ **Theory 30Marks** • Class Participation: **5 Marks** • Seminar/presentation/assignment/quiz/class test etc.:**10Marks** • Mid-Term Exam: **15Marks**	**End Term Examination: 70 Marks**

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. Microelectronic Processing: An Introduction to the Manufacture of Integrated Circuits by W. Scot Ruska (McGraw Hill International Edition).
2. VLSI Technology by S. M. Sze (2nd Edition)
3. Microchip Fabrication: A Practical Guide to Semiconductor Processing by Peter Van Zant (2nd Edition) (McGraw Hill Publishing Company).
4. Vacuum Technology by A. Roth
5. Semiconductor Devices: Physics and Technology by S.M. Sze.
6. VLSI Fabrication Principles: Silicon and Gallium Arsenide by Sorab K. Ghandhi (John Wiley & Sons).

Session:2025-26			
Part A - Introduction			
Subject	ELECTRONIC EQUIPMENT MAINTENANCE		
Semester	SEVENTH		
Contact Hours	Electronic Communication-3		
Course Code	B23-EEM-703		
Course Type: (CC/MCC/MDC/CC-M/DSEC/VOC/DSE/PC/AEC/VAC)	CC-H3		
Level of the course	400-499		
Pre-requisite for the course (if any)	Basic knowledge of Electronics.		
Course Learning Outcomes (CLO):	After completing this course, the learner will be able to: 1. Explain wave equation and boundary conditions 2. Understand the radio waves and analyze Smith chart for impedance matching 3. Explain various pulse and digital modulation techniques. 4. Understand the basics of modern telephone network and satellite communication		
Credits	Theory	Practical	Total
	4	-	4
Contact Hours	60	-	60
Max. Marks: 100 Internal Assessment Marks: 30 End Term Exam Marks:70		Exam Time: 3 Hours	

Part B - Contents of the Course

Instructions for Paper-Setter

1. Nine questions will be set in all. All questions will carry equal marks.
2. Question No.1, which will be short answer type covering the entire syllabus, will be compulsory. The remaining eight questions will be set unit wise selecting two questions from each Unit I to IV. The candidate will be required to attempt question No. 1 and four more questions selecting one question from each unit

Unit	Topics	Contact Hours
I	Wave Equation and Boundary conditions, Plane monochromatic wave in non-conducting media, conducting media, Reflection and refraction at the boundary of two non-conducting media-oblique incidence, Reflection from a conducting plane-total internal reflection, Propagation between parallel conducting plates, Radio Wave propagation: Propagation in Free space, Tropospheric Propagation, Ionospheric propagation, Surface wave propagation, Propagation losses	**15**
II	Transmission lines, Characteristic impedance, standing waves, quarter and half wavelength lines, Impedance matching, Use of Smith Chart, Impedance matching using Smith Chart, Losses in Transmission lines, Wave-guides: Rectangular, losses in Wave-guides, S Parameters, Basics of Antennas: Antenna parameters, Dipole antennas, Radiation pattern, Antenna gain.	**15**
III	Pulse Communication, Pulse Amplitude modulation (PAM), Pulse Width Modulation, Pulse Position Modulation (PPM), Pulse Code Modulation and application. Digital Communication, Characteristics of Data Transmission Circuit, Data Transmission speeds, Noise, Cross talks, Echo suppressors, Distortion, Equalizers, Bit transmission, Signaling rate, Digital Communication techniques, FSK, PSK, BPSK, QPSK, DPSK. Error Detection and Correction codes.	**15**

IV	Modern Telephone networks, mobile telephone network, intelligent network and services (in brief). Satellite Communication: Introduction, Orbits, Station keeping, Satellite Attitude, Transmission Path, Path Loss, Noise considerations, the Satellite Systems, Saturation flux density, Effective Isotropic radiated Power, Multiple Access Methods.	**15**

Suggested Evaluation Methods

Internal Assessment: ➢ **Theory 30Marks** • Class Participation: **5 Marks** • Seminar/presentation/assignment/quiz/class test etc.:**10Marks** • Mid-Term Exam: **15Marks**	**End Term Examination:** **70 Marks**

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. Foundations of Electromagnetic Theory JR Reitz and FZ by Reitz and Milford (Addison Wesley).
2. Electromagnetics by B.B. Laud (Wiley Eastern).
3. Mathew N. O. Sadiku, 'Principles of Electromagnetics', 6th Edition, Oxford University Press Inc. Asian edition, 2015.
4. Theory and Applications of Microwaves by Brownwell and Beam (McGraw Hill).
5. Electronic Communication by George Kennedy.
6. Basic Electronic Communication by Roody & Coolen.
7. Electronic Communications System by Wayne Tomasi (Pearson).

Session: 2025-26			
Part A - Introduction			
Subject	ELECTRONIC EQUIPMENT MAINTENANCE		
Semester	SEVENTH		
Contact Hours	Instrumentation and Control System		
Course Code	B23-EEM-704		
Course Type: (CC/MCC/MDC/CC-M/DSEC/VOC/DSE/PC/AEC/VAC)	DSE- H1		
Level of the course	400-499		
Pre-requisite for the course (if any)			
Course Learning Outcomes (CLO):	After completing this course, the learner will be able to: 1.Understand the characteristics of sensors and transducers and analyze their performance 2.Understand different methods for measuring a physical quantity and role of different instrumentation required for measuring the same 3.Identify different control systems, analyze using SFG and design these for specified purpose 4.Use different techniques to perform stability analysis of the designed control system and capability to do the state space analysis		
Credits	Theory	Practical	Total
	4	-	4
Contact Hours	60	-	60
Max. Marks: 100 Internal Assessment Marks: 30 End Term Exam Marks:70		Exam Time: 3 Hours	

Part B-Contents of the Course

Instructions for Paper-Setter

1. Nine questions will be set in all. All questions will carry equal marks.
2. Question No.1, which will be short answer type covering the entire syllabus, will be compulsory. The remaining eight questions will be set unit wise selecting two questions from each Unit I to IV. The candidate will be required to attempt question No. 1 and four more questions selecting one question from each unit

Unit	Topics	Contact Hours
I	Basic concepts of measurement: Introduction, system configuration basic characteristics of measuring devices, Transducer Classification :Introduction, Electrical transducer, classification, basic requirements, Performance characteristics of an instrumentation system: generalized system, zero order, first order, second order system, Measurement of displacement: principle of transduction, Variable resistance device, LVDT, Variable capacitance transducer, Hall effect devices, Measurement of pressure: Thin film pressure transducer, piezoelectric pressure transducer vibrating element pressure transducer	**15**
II	Measurement of position, velocity, force, torque (basics only), Measurement of flow: Head type flow meters based on differential pressure measurements, Anemometers, Temperature measurements: resistance type temp. sensors, thermistors, thermocouples, solid state sensors, optical pyrometers, Measurement of humidity, thickness, pH (basics only), Instrumentation amplifier, Q meter, Digital storage oscilloscope, Lock-in Amplifier.	**15**

III	Bioelectrical signals and their measurement, Electrodes for ECG **Control System:** Introduction: Basic components of a control system, Example of control system applications, Open loop and closed loop control system, Feedback and its effects, Types of feedback control systems, Transfer functions, block diagram, and Signal Flow graphs. Time response of feedback control systems: Steady state error analysis, Introduction and design of P, I PI, PD and PID Controllers .	**15**
IV	Stability of linear control systems: introduction, Methods of determining stability, Routh –Hurwitz stability, Nyquist Stability Criterion, Root loci technique for analysis of LTI control system, Bode plots and Nyquist plots. **Introduction to State variable analysis:** Concepts of state, state variable and state models for electrical systems, Solution of state equations.	**15**

Suggested Evaluation Methods

Internal Assessment: ➢ **Theory 30Marks** • Class Participation: **5 Marks** • Seminar/presentation/assignment/quiz/class test etc.:**10Marks** • Mid-Term Exam: **15Marks**	**End Term Examination:** **70Marks**

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. Modern Electronic Instrumentation and Measurement Technique by Alfred D. Helfrick and William D. Cooper, (Eastern Economy Edition)
2. Instrumentation Devices and Systems by C.S. Rangan, G.R. Sarma and V.S.V Mani, Tata McGraw Hill .
3. Principles of Measurement and Instrumentation by Alan S. Morris, Prentice Hall.
4. Automatic Control Systems by Benjamin C. Kuo, Prentice Hall India.
5. Modern Control Engineering by K. Ogata, PHI.
6. Bio-Medical Instrumentation by R.S Khandpur.

Session: 2025-26			
Part A - Introduction			
Subject	ELECTRONIC EQUIPMENT MAINTENANCE		
Semester	SEVENTH		
Contact Hours	CAD Tools for Microelectronics		
Course Code	B23-EEM-705		
Course Type: (CC/MCC/MDC/CC-M/DSEC/VOC/DSE/PC/AEC/VAC)	DSE-H1		
Level of the course	400-499		
Pre-requisite for the course (if any)			
Course Learning Outcomes (CLO):	After completing this course, the learner will be able to: 1. Study various physical design methods in VLSI. 2. Understand the concepts behind the VLSI design rules and routing techniques. 3. Use the simulation techniques at various levels in VLSI design flow. 4. To understand the concepts of various algorithms used for floor planning and routing• techniques.		
Credits	Theory	Practical	Total
	4	-	4
Contact Hours	60	-	60
Max. Marks: 100 Internal Assessment Marks: 30 End Term Exam Marks:70		Exam Time: 3 Hours	

Part B - Contents of the Course

Instructions for Paper-Setter

1. Nine questions will be set in all. All questions will carry equal marks.
2. Question No.1, which will be short answer type covering the entire syllabus, will be compulsory. The remaining eight questions will be set unit wise selecting two questions from each Unit I to IV. The candidate will be required to attempt question No. 1 and four more questions selecting one question from each unit

Unit	Topics	Contact Hours
I	**VLSI DESIGN METHODOLOGIES:** Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable problems - general purpose methods for combinatorial optimization	**14**
II	**DESIGN RULES :** Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation - Placement algorithms – partitioning	**14**
III	**FLOOR PLANNING**: Floor planning concepts - shape functions and floor plan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.	**14**
IV	**SIMULATION :** Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis. **MODELLING AND SYNTHESIS** : High level Synthesis - Hardware models - Internal representation - Allocation - assignment and scheduling - Simple scheduling algorithm - Assignment problem - High level transformations.	**18**

Suggested Evaluation Methods	
Internal Assessment: ➢ **Theory 30Marks** • Class Participation: **5 Marks** • Seminar/presentation/assignment/quiz/class test etc.:**10Marks** • Mid-Term Exam: **15Marks**	**End Term Examination: 70Marks**

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2002.
2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.
3. Sadiq M. Sait, Habib Youssef, “VLSI Physical Design automation: Theory and Practice”, World scientific 1999.
4. Steven M.Rubin, “Computer Aids for VLSI Design”, Addison Wesley Publishing 1987.

Session: 2025-26			
Part A - Introduction			
Subject	ELECTRONIC EQUIPMENT MAINTENANCE		
Semester	SEVENTH		
Contact Hours	Practicals Based on B23-EEM-701 to 704/705		
Course Code	B23-EEM-706		
Course Type: (CC/MCC/MDC/CC-M/DSEC/VOC/DSE/PC/AEC/VAC)	PC-H1		
Level of the course	400-499		
Pre-requisite for the course(if any)			
Course Learning Outcomes (CLO):	After completing this course, the learner will be able to: 1.Design analog electronics circuits based on semiconductor devices (Diode/BJT/MOSFET). 2.Present the experimental results and conclusions in the form of written report in clear and concise manner 3.Design combinational and sequential circuits using CMOS devices/ICs 4.Write a program/code using high level computer language for solving scientific problems 5.Analyse & interpret the data obtained in the experiments 6.Present the experimental results and conclusions in the form of written report in clear and concise manner		
Credits	**Theory**	**Practical**	**Total**
	-	4	4
Contact Hours	-	60	60
Max. Marks: 100 Internal Assessment Marks: 30 End Term Exam Marks:70		Exam Time: 3 Hours	

Part B-Contents of the Course

Instructions for Performing the Experiment

Note: Perform ten practicals selecting at least one from Practicals Based on B23-EEM-701 to 704/705

1. Familiarization with electronic instruments like CRO, Multimeter, Function Generator etc.
2. Bipolar Junction Transistor based Amplifier Design (with & without Feedback)
3. Plot MOSFET characteristics and design common source amplifier.
4. Design of Analog Multimeter
5. IC 555 applications: Monoshot, Astable, Bistable Multivibrator, Schmitt Trigger etc,
6. OP- AMP based applications: Sample and hold circuits, logarithmic amplifier precision rectf.
7. OP- AMP Waver form generator, Triangular, Square & sine waver generators
8. Op- Based Active filters (IInd Order) – Low Pass, High Pass, Band Pass, Band Reject
9. Familiarization with Vaccum System and metal film deposition using thermal evaporation.
10. Wafer cleaning and verification of wafer type
11. Familiarization with Study of CMOS digital ICs families.
12. Design of digital inverter circuits using BJT devices and find out the noise margins from the transfer curve.
13. Design of synchronous and asynchronous digital counters.
14. Implementation of half adder and full adder circuit using CMOS digital ICS.
15. A/D and D/A converter circuits.
16. C-Programming- logical, arithmetic, decision making and loop operations.
17. C-Programming- file operations, functions & subroutines.

18. C-Programming- numerical methods
19. Plot device characteristics using C programs
20. Programming using MATLAB
21. Design of the combinational circuits using PLAs
22. Design of the combinational/sequential circuits using PLDs.
23. VHDL program on Full Adder Data Flow Modeling
24. VHDL Program for 8:1 MUX/1:8 DEMUX
25. VHDL Program for Priority Encoder (8:3)
26. Simple project (Any topic related to the scope of the Practical course)

Suggested Evaluation Methods

Internal Assessment:30 Marks • Class Participation: 10Marks • File Preparation: 5 Marks • Viva/Seminar/ Quiz/Assignments: 15 Marks	**End Term Examination:** 70 Marks

Session: 2025-26			
Part A - Introduction			
Subject	ELECTRONIC EQUIPMENT MAINTENANCE		
Semester	EIGHT		
Name of the Course	CMOS and PLD Logic Design		
Course Code	B23-EEM-801		
Course Type: (CC/MCC/MDC/CC-M/DSEC/VOC/DSE/PC/AEC/VAC)	CC-H4		
Level of the course	400-499		
Pre-requisite for the course(if any)	Knowledge of Basic electronics circuits and components		
Course Learning Outcomes (CLO):	After completing this course, the learner will be able to: 1.Understand and compare different CMOS logic families 2.Understanding of different types of CMOS PLDs and implementation of basic circuits in VHDL 3.Analyze and design of State Machines 4.Define Impediments to Synchronous Design Methodology		
Credits	Theory	Practical	Total
	4	-	4
Contact Hours	60	-	60
Max. Marks: 100 Internal Assessment Marks: 30 End Term Exam Marks:70		Exam Time: 3 Hours	

Part B-Contents of the Course

Instructions for Paper-Setter

1. Nine questions will be set in all. All questions will carry equal marks.
2. Question No.1, which will be short answer type covering the entire syllabus, will be compulsory. The remaining eight questions will be set unit wise selecting two questions from each Unit I to IV. The candidate will be required to attempt question No. 1 and four more questions selecting one question from each unit.

Unit	Topics	Contact Hours
I	Introduction to CMOS Circuits, Logic families, CMOS logic, Electrical behaviour of CMOS circuits, CMOS steady state electrical behaviour, CMOS dynamic electrical behaviour, CMOS Input and Output structures, CMOS logic families, CMOS/TTL interfacing, Timing Hazards, Quine-McCluskey Method of finding Minimal SOP and POS Expressions.	**15**
II	Combinational Logic Design Practice: Documentation standards, circuit timing, Combinational PLDs: Programmable logic array (PLA), Implementation of combinational logic using PLA, Programmable array logic (PAL), Generic Array logic (GAL), Description of some basic PLDs, Complex Programmable Logic Devices (CPLDs), Combinational PLD applications. Implementation of following in VHDL decoders, encoders, three state devices, multiplexers, exclusive-OR gates and parity circuits, comparators, adders, combinational multipliers.	**15**
III	Bistable elements, Latches and Flip-Flops, Clocked Synchronous State-machine Analysis, Clocked Synchronous State- machine Design, Designing State Machines using State Diagrams, State-machine Synthesis using Transition Lists.	**15**

IV	Sequential PLDs, Registers: Shift Registers and counters, Iterative versus Sequential Circuits, Synchronous Design Methodology, Impediments to Synchronous Design, Synchronizer Failure and Meta stability, Field Programmable Gate Arrays.	**15**

Suggested Evaluation Methods

Internal Assessment: ➢ **Theory 30Marks** • Class Participation: **5 Marks** • Seminar/presentation/assignment/quiz/class test etc.:**10Marks** • Mid-Term Exam: **15Marks**	**End Term Examination:** **70 Marks**

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. Digital Design: Principles & Practices-John F. Wakerly (4th edition, Prentice Hall).
2. Programmable Logic: PLDs and FPGAs- R.C. Seals, G.F. Whapshott (McGraw-Hill, Publication)

Session: 2025-26			
Part A - Introduction			
Subject	ELECTRONIC EQUIPMENT MAINTENANCE		
Semester	EIGHT		
Name of the Course	MOS Device Modeling and CMOS Amplifier Design		
Course Code	B23-EEM-802		
Course Type: (CC/MCC/MDC/CC-M/DSEC/VOC/DSE/PC/AEC/VAC)	CC-H5		
Level of the course	400-499		
Pre-requisite for the course(if any)			
Course Learning Outcomes (CLO):	After completing this course, the learner will be able to: 1.Describe the mathematical models for semiconductor devices and use it for circuit simulation. 2.Design various analog building blocks like switches, current mirrors and active resistors using MOSFET devices. 3.Analyze the performance of MOSFET based amplifier systems in integrated circuits. 4. Differentiate between various configurations of op-amp in terms of performance of Integrated Circuits..		
Credits	**Theory**	**Practical**	**Total**
	4	-	4
Contact Hours	60	-	60
Max. Marks: 100 Internal Assessment Marks: 30 End Term Exam Marks:70		Exam Time: 3 Hours	

Part B-Contents of the Course

Instructions for Paper-Setter

1. Nine questions will be set in all. All questions will carry equal marks.
2. Question No.1, which will be short answer type covering the entire syllabus, will be compulsory. The remaining eight questions will be set unit wise selecting two questions from each Unit I to IV. The candidate will be required to attempt question No. 1 and four more questions selecting one question from each unit.

Unit	Topics	Contact Hours
I	Device Modeling, DC models, small signal models, use of device models in circuit analysis, diode models, dc diode model, small signal diode model, HF diode model, MOS models, large signal (or dc) MOSFET model, small signal MOSFET model, HF MOSFET model, short channel Devices, sub-threshold MOS Models, Modeling noise sources in MOSFET's. MOS Device Layouts, Circuit simulation, Circuit simulation using SPICE, MOS SPICE Models,	**15**
II	MOS switches, MOS Diode/active resistors, Current sources and sinks, Basic Current Mirrors, Cascoded Current Mirror, Widlar & Wilson Current mirror CMOS amplifiers: Single stage MOS Inverting Amplifier with various load configurations (resistive, diode connected, and current source as load), CMOS Push Pull amplifier	**15**
III	Differential amplifiers: Qualitative and quantitative analysis, CMOS differential amplifiers -Differential pair with active loads, Differential pair with current source and current mirror load, Frequency response of Amplifiers: Concept of zeros and poles, Miller effect, Association of poles with nodes, frequency response of MOS inverting amplifiers and differential amplifiers.	**15**

IV	CMOS two stage OP Amp, Stability and frequency compensation, Multipole system, Concept of phase margin, frequency compensation, compensation of two stage op-amp Simulation and measurement of op-amps, Comparators, characterization of comparators, High gain comparators, Propagation delay of two-stage comparators, Comparators using positive feedback, Autozeroing.	**15**

Suggested Evaluation Methods

Internal Assessment: ➢ **Theory 30Marks** • Class Participation: **5 Marks** • Seminar/presentation/assignment/quiz/classtestetc.:**10Marks** • Mid-TermExam: **15Marks**	**End Term Examination: 70Marks**

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. Design of analog CMOS Integrated Circuits, Behzad Razavi, Tata McGraw Hill
2. VLSI Design Techniques for Analogue and Digital Circuits by R.L. Geiger, P.E. Allen and N.R. Strader.
3. Analysis and Design of Analogue I.C's (2nd edition) by P.R. Gray, R.G. Meyer.
4. The SPICE book by Andrei Vladimirescu.
5. Computer Simulation of Electronic Circuits by Raghuram.

Session: 2025-26			
Part A - Introduction			
Subject	ELECTRONIC EQUIPMENT MAINTENANCE		
Semester	EIGHT		
Contact Hours	Verilog Hardware Description Language		
Course Code	B23-EEM-803		
Course Type: (CC/MCC/MDC/CC-M/DSEC/VOC/DSE/PC/AEC/VAC)	CC-H6		
Level of the course	400-499		
Pre-requisite for the course (if any)			
Course Learning Outcomes (CLO):	After completing this course, the learner will be able to: 1.Understand the basics of Verilog Hardware Description Language 2.Design Verilog models for digital circuits using Gate level, Dataflow and Switch level modelling 3.Design Verilog models for digital circuits using behavioural level modelling, and using Generate blocks, tasks and functions 4.Use delays, UDPs and the concept of synthesis and verification in Verilog models		
Credits	Theory	Practical	Total
	4	-	4
Contact Hours	60	-	60
Max. Marks: 100 Internal Assessment Marks: 30 End Term Exam Marks:70		Exam Time: 3 Hours	

Part B - Contents of the Course

Instructions for Paper-Setter

1. Nine questions will be set in all. All questions will carry equal marks.
2. Question No.1, which will be short answer type covering the entire syllabus, will be compulsory. The remaining eight questions will be set unit wise selecting two questions from each Unit I to IV. The candidate will be required to attempt question No. 1 and four more questions selecting one question from each unit.

Unit	Topics	Contact Hours
I	Benefits of CAD, Integrated circuit design techniques, Hierarchical design, Design abstraction, Computer aided design, Concepts of CPLD, FPGA. Introduction to HDLs, Verilog and its capabilities, Hierarchical Modeling Concepts: Design Methodologies, Modules, Instances, Components of Simulation and Test Bench. Basic Concepts: Lexical Conventions, Data Types, System Tasks and Compiler Directives. Modules and Ports.	**15**
II	Gate-Level Modeling: Gate Types, Gate Delays. Dataflow Modeling, Continuous Assignments, Delays, Expressions, Operators, and Operands, Operator Types, Switch-Level Modeling: Switch-Modeling Elements.	**15**
III	Behavioral Modeling: Structured Procedures, Procedural Assignments, Timing Controls, Conditional Statements, Multiway Branching, Loops, Sequential and Parallel Blocks, Generate Blocks. Tasks and Functions.	**15**

IV	Timing and Delays, Types of Delay Models, Path Delay Modeling, Timing Checks, Delay Back-Annotation, User-Defined Primitives (brief), Programming Language Interface (brief), Logic Synthesis with Verilog, Synthesis Design Flow, Verification of Gate-Level Netlist. Verification Techniques (brief) : Traditional Verification Flow, Assertion Checking, Formal Verification	**15**

Suggested Evaluation Methods

Internal Assessment: ➢ **Theory 30Marks** • Class Participation: **5 Marks** • Seminar/presentation/assignment/quiz/class test etc.:**10Marks** • Mid-Term Exam: **15Marks**	**End Term Examination: 70Marks**

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. Custom VLSI Microelectronics by Stanley L.Hurst (Prentice Hall 1992)
2. Verilog HDL - Samir Palnitkar (Pearson)
3. A Verilog HDl Primer - J. Bhaskar (Pearson)
4. Modern VLSI Design- A Systems Approach- Wayne Wolf-PTR Prentice Hall-1994

Session: 2025-26			
Part A - Introduction			
Subject	ELECTRONIC EQUIPMENT MAINTENANCE		
Semester	EIGHT		
Contact Hours	Embedded Systems Design		
Course Code	B23-EEM-804		
Course Type: (CC/MCC/MDC/CC-M/DSEC/VOC/DSE/PC/AEC/VAC)	DSE-H2		
Level of the course	400-499		
Pre-requisite for the course (if any)	NIL		
Course Learning Outcomes (CLO):	After completing this course, the learner will be able to: 1.Understand need and applications of the Embedded Systems 2.Analyse given problem and write programs using 8051 assembly language 3.Design interfacing circuits using standard peripherals 4.Understand the issues with hardware-software co-design		
Credits	Theory	Practical	Total
	4	-	4
Contact Hours	60	-	60
Max. Marks: 100 Internal Assessment Marks: 30 End Term Exam Marks:70		Exam Time: 3 Hours	

Part B-Contents of the Course

Instructions for Paper-Setter

1. Nine questions will be set in all. All questions will carry equal marks.
2. Question No.1, which will be short answer type covering the entire syllabus, will be compulsory. The remaining eight questions will be set unit wise selecting two questions from each Unit I to IV. The candidate will be required to attempt question No. 1 and four more questions selecting one question from each unit.

Unit	Topics	Contact Hours
I	**Introduction to Embedded Systems** : what is an Embedded system? , Embedded Systems vs General Computing Systems, Classification, major application areas, purpose of Embedded Systems, Wearable devices as an example of Embedded Systems **The Typical Embedded system** : Core of Embedded System, Memory, Sensors and Actuators, Communication Interface, Embedded Firmware, other system components	**15**
II	Characteristics and Quality Attributes of Embedded Systems, Washing machine as application specific Embedded System and Automotive as domain specific embedded system **Designing Embedded Systems with 8bit Microcontrollers-8051:** controller selection, why 8051? **Designing with 8051 Microcontroller :** 8051 architecture, Memory Organization, Oscillator Unit, Ports, Interrupts, Timer Units, Serial Port, Reset Circuitry, Power saving modes	**15**

III	**Programming the 8051 Microcontroller :** Addressing modes , Instruction Set – Data transfer, Arithmetic,Logical Instructions, Boolean Instructions, Program Control Transfer Instructions, **ALP for implementation of Instruction set** :binary to unpacked BCD, data transfer to internal and external memory, delay using timers **Design Examples** :number display on LED, 7-segment display, stepper motor control, Analog to Digital Converter Interfacing, serial data transmission.	**15**
IV	**Hardware-Software Co-Design and Program Modelling :** Issues in Hardware-Software Co-Design, Computational Models in Embedded Systems, Introduction to Unified Modelling Language.	**15**

Suggested Evaluation Methods

Internal Assessment: ➢ **Theory30Marks** • Class Participation: **5 Marks** • Seminar/presentation/assignment/quiz/class test etc.:**10Marks** • Mid-Term Exam: **15Marks**	**End Term Examination:70 Marks**

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. Semiconductor Material and Device Characterization-Dieter K.Schroder (John Wiley & Sons).
2. Technique of Physics Vol.13, The Electrical Characterization of Semiconductors, Measurement of Minority carrier Properties-J.W.Octon and P.Blood (Academic Press)
3. VLSI Technology-S.M.Sze (McGraw Hill Publications).
4. Nano – A Perspective – T.Pradeep (TMH)

Session: 2025-26			
Part A - Introduction			
Subject	ELECTRONICS		
Semester	EIGHT		
Contact Hours	Advanced Digital Communication Systems		
Course Code	B23-EEM-805		
Course Type: (CC/MCC/MDC/CC-M/DSEC/VOC/DSE/PC/AEC/VAC)	DSE-H2		
Level of the course	400-499		
Pre-requisite for the course (if any)			
Course Learning Outcomes (CLO):	After completing this course, the learner will be able to: 1. Understand the concepts of building blocks and theoretical concepts of digital communication system. 2. Develop essential design concepts of each of the blocks of digital communication system 3. Understand various techniques for digital transmission of analog signals and multiple access techniques for data transmission		
Credits	Theory	Practical	Total
	4	-	4
Contact Hours	60	-	60
Max. Marks: 100 Internal Assessment Marks: 30 End Term Exam Marks:70		Exam Time: 3 Hours	

Part B-Contents of the Course

Instructions for Paper-Setter

1. Nine questions will be set in all. All questions will carry equal marks.
2. Question No.1, which will be short answer type covering the entire syllabus, will be compulsory. The remaining eight questions will be set unit wise selecting two questions from each Unit I to IV. The candidate will be required to attempt question No. 1 and four more questions selecting one question from each unit.

Unit	Topics	Contact Hours
I	Introduction :Model of Communication System, Elements of a Digital Communication System, Analysis and Design of Communication System, Classification of Signals and Systems A brief review of Random Signal Theory : Probabilities, Random Variables and Random Processes Information and Channel Capacity : Measure of Information, Encoding of the Source output – Shannon Encoding Algorithm and Huffman Encoding algorithm (Ref. 3), Discrete Communication Channels : Only Memory less, Continuous Communication Channel : Shannon- Hartley Theorem	**15**
II	Digital Modulation Techniques: Introduction, Binay Phase-Shift Keying, Differential Phase-Shift Keying, Differentially- Encoded PSK, Quardrature Phase Shift Keying, M-ary PSK, Quadrature Amplitude Shift Keying, Binary FSK, Similarity of BFSK and BPSK, M-ary FSK, Minimum Shift Keying, Duobinary Encoding, A Comparison of Narrowband FM System (Ref 2)	**15**
III	Error control coding: Examples of Error control coding, Methods of controlling errors, Types of errors and codes, Linear block codes, Binary cyclic codes. Convolutional Codes-Trellis Code	**15**

IV	Digital Transmission of Analog Signals, Sampling theory and Practice, Quantizing of Analog Signals, , PCM, Delta Modulation, Q-level differential PCM, Time DivisionMultiplexing, Spread Spectrum and Multiple Access Techniques, Introduction to Spread Spectrum Modulation , Code Acquisition and Tracking , Spread Spectrum as a Multiple Access Techniques..	**15**

Suggested Evaluation Methods

Internal Assessment: ➢ **Theory30Marks** • Class Participation: **5 Marks** • Seminar/presentation/assignment/quiz/class test etc.:**10Marks** • Mid-Term Exam: **15Marks**	**End Term Examination:70 Marks**

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. Digital and Analog Communication Systems by K. Sam Shanmugan (John wiley& Sons 1994).
2. Principles of Communication System by Taub and Schilling (McGraw Hill International).
3. An Introduction to Analog& Digital Communication by Simon Haykin.
4. John G.Proakis, "Digital Communication" McGraw Hill 3rd Edition, 1995

Session: 2025-26			
Part A - Introduction			
Subject	ELECTRONIC EQUIPMENT MAINTENANCE		
Semester	EIGHT		
Name of the Course	Practical Based on B23-EEM-801 to 804/805		
Course Code	B23-ELE-806		
CourseType:(CC/MCC/MDC/CC-M/DSEC/VOC/DSE/PC/AEC/VAC)	PC-H2		
Level of the course	400-499		
Pre-requisite for the course(if any)			
Course Learning Outcomes (CLO):	After completing this course, the learner will be able to: Get the Hands on experiments and their analysis based on the knowledge of different experiments based on B23-EEM-801-804/805: 1.Perform the simulation of analog electronic circuits involving BJT/MOSFET Devices using LTSPICE and Cadence Tools 2.Be proficient in use of IDE's for designing, testing of microcontroller-based system 3.Analyze & interpret the data obtained in the experiments 4. Present the experimental results and conclusions in the form of written report in clear and concise manner 5. To measure the parameters of semiconductor materials and device. 6. To use the techniques and equipment used for fabrication of semiconductor devices and integrated circuits. 7. To Analyze and interpret experimental data 8. Present the experimental results and conclusions in the form of written report in clear and concise manner		
Credits	**Theory**	**Practical**	**Total**
	0	4	4
Contact Hours	0	60	60
Max. Marks: 100 Internal Assessment Marks: 30 End Term Exam Marks:70		Exam Time: 3 Hours	

Part B-Contents of the Course

Instructions for Performing the Experiments

Note: Perform ten experiments selecting at least one from Practicals Based on B23-EEM-801 to 804/805

1. CMOS inverting Amplifier Circuits simulation using EDA Tools (Cadence Tools)
2. CMOS Differential Amplifiers with Active Loads using EDA Tools
3. Design and simulation of MOS Current sources
4. Design and Simulation of Current Mirror Circuits (Cascoded/Widler/Wilson)
5. Design and Simulation of first and second order Active Filter Circuits.
6. TCAD Simulation of semiconductor devices and processes.
7. Simulation of MEMS structures
8. Programming of 8051 using data flow instructions
9. Programming of 8051 using jump instructions
10. Use of external memories using 8051
11. Study of Hall Effect
12. Resistivity measurement using four probe setup
13. Study of PN junction parameters
14. Study of optoelectronic devices and solar cell
15. Characteristics of semiconductor power devices: UJT and SCR
16. Oxidation of silicon wafers (both wet & Dry) and oxide thickness measurement

17. Pattern transfer using photolithography (using positive photoresist)
18. Wet etching of oxide and Aluminum film
19. Metal-Semiconductor Contact Fabrication & characterization
20. MOS Fabrication & its CV Characterization

Suggested Evaluation Methods

Internal Assessment:30 Marks • Class Participation: 10Marks • File Preparation: 5 Marks • Viva/Seminar/ Quiz/Assignments: 15 Marks	**End Term Examination:** 70 Marks