Kurukshetra University, Kurukshetra

(Established by the State Legislature Act-XII of 1956)
("A++" Grade, NAAC Accredited)

Syllabus
for

Post Graduate Programme

M.Sc Electronic Science

3rd & 4th Semester

as per NEP 2020
Curriculum and Credit Framework for Postgraduate Programme

With CBCS-LOCF
With effect from session 2025-2026

DEPARTMENT OF ELECTRONIC SCIENCE
FACULTY OF SCIENCE

KURUKSHETRA UNIVERSITY, KURUKSHETRA -136119
HARYANA, INDIA

w.e.f. session 2025-26			
Part A - Introduction			
Name of Programme	M.Sc. Electronic Science		
Semester	Third		
Name of the Course	MOS Solid State Circuits		
Course Code	M24-ELE-301		
Course Type	CC-9		
Level of the course	500-599		
Pre-requisite for the course	M24-ELE-101		
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO 1 : Describe the working principals of basic building blocks of digital systems CLO 2 : Explain the functioning of dynamic storage like DRAMs and binary adders circuits CLO 3 : Estimate the various MOS capacitances and delays present in the integrated circuits CLO 4: Use various testing and simulation methods used in integrated circuits.		
Credits	Theory	Practical	Total
	4	0	4
Teaching Hours per week	4	0	4
Internal Assessment Marks	30	0	30
End Term Exam Marks	70	0	70
Max. Marks	100	0	100
Examination Time	3 hours		

Part B- Contents of the Course

Instructions for Paper- Setter: The examiner will set 9 questions asking two questions from each unit and one compulsory question by taking course learning outcomes (CLOs) into consideration. The compulsory question (Question No. 1) will consist at least 4 parts covering entire syllabus. The examinee will be required to attempt 5 questions, selecting one question from each unit and the compulsory question. All questions will carry equal marks.

Unit	Topics	Contact Hours	CLOs
I	Basic digital building blocks, NMOS inverter and its sizing rules, single input NMOS NOR and NAND logic circuits, CMOS inverters, CMOS NOR logic gate, CMOS NAND logic gate, power dissipation , CMOS AND NMOS power dissipation, latch-up and its prevention, signal propagation delays, ratio-logic models, inverter pair delay, NMOS,NAND and NOR delays, CMOS logic delays.voltage.	15	CLO1
II	Dynamic MOS storage circuits, dynamic charge storage, simple shift register, clocked CMOS logic, dynamic RAM memory, register storage circuits, datapath operators, bitparallel adders, bit-serial adders, carry-save addition, pipelining, pipeline architecture, Floor planning methods, block placement and channel definition, routing, power distribution.	15	CLO2
III	Layout Design rules, resistance estimation, capacitance estimation, MOS capacitor characteristics, MOS device capacitances, diffusion capacitances, single wire capacitance, capacitance design guide, inductance estimation, analytical delay models, gate delay model, power dissipation, static and dynamic power dissipation, shortcircuit dissipation, total power dissipation.	16	CLO3
IV	CMOS tests methods, need for testing, functionality tests, manufacturing tests and principles, fault models, stuck-at faults, short-circuit and open-circuit faults, Automatic test pattern generation, geometrical specification	14	CLO4

	languages, parameterized layout representation, graphical symbolic layout, layout equation symbology, design rule checks, digital circuit simulation, logic level simulation, switch level simulation, RTL level simulation.		
		Total Contact Hours	60

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. VLSI Design Techniques for Analog and Digital Circuits by Randall L. Geiger, Phillip E. Allen and Noel R. Strader, McGraw-Hill.
2. Principles of CMOS VLSI Design- A System Perspective by Neil H.E. Weste and Kamrin Eshraghin, Second Edition, Addison-Wesley.
3. Modern VLSI design – System –on-Chip Design by Wayne Wolf, PHI, Third Edition.
4. Fundamentals of Digital Logic Design by Pucknell (P.Hall)

Evaluation Method

Outcomes	**Internal Assessment (30 Marks)**			**End Semester Examination (70 Marks)**
	Mid Term Exam	Seminar/Presentation/ Assignment/Quiz/Test	**Class Participation**	**SEE**
Marks :	**15**	**10**	**5**	**70**
CLO1	5	-	-	15
CLO2	5	2.5	-	20
CLO3	5	2.5		20
CLO4		5		15

w.e.f. Session: 2025-26			
Part A - Introduction			
Name of Programme	M.Sc. Electronic Science		
Semester	Third		
Name of the Course	Optoelectronics & Microwave Devices		
Course Code	M24-ELE-302		
Course Type	CC-10		
Level of the course	500-599		
Pre-requisite for the course	NIL		
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO1: Explain the basic microwave parameters and working of passive and active components. CLO2: Understand the working of microwave solid state devices. CLO3: Understand the structure and working of display devices including LED, Laser CLO4: Understand quantum well based devices the working of various detectors and fibers used in fibre- optic communication		
Credits	Theory	Practical	Total
	4	0	4
Teaching Hours per week	4	0	4
Internal Assessment Marks	30	0	30
End Term Exam Marks	70	0	70
Max. Marks	100	0	100
Examination Time	3 hours		

Part B- Contents of the Course

Instructions for Paper- Setter: The examiner will set 9 questions asking two questions from each unit and one compulsory question by taking course learning outcomes (CLOs) into consideration. The compulsory question (Question No. 1) will consist at least 4 parts covering entire syllabus. The examinee will be required to attempt 5 questions, selecting one question from each unit and the compulsory question. All questions will carry equal marks.

Unit	Topics	Contact Hours	CLOs
I	Microwave Introduction, Waveguides, Rectangular Waveguides - excitation of modes, power transmission, power losses, Microwave parameters-cut off frequency, Characteristic Impedance, Attenuation constant, Phase, Reflection Coefficient, SWR, Power. Microwave passive components (brief)-discontinuities, bands, flanges, TEE's, directional coupler, matched load, attenuators, phase shifter, transitions, ferrite components, slotted line, Wavemeter. Measurements of wavelength, Frequency, impedance, SWR etc. Rectangular Cavity Resonator, Q of cavity, Reentrant cavities. Klystron-operation, velocity modulation, Reflex Klystron-operation, velocity modulation.	15	CLO1
II	Traveling wave tube (in brief), Planar Triodes. Magnetrons (in brief). Transferred Electron Devices, Gunn Effect diode-operation, Modes of operation, microwave generation, amplification, Avalanche Transit Time Devices (in brief). - IMPATT diode, TRAPATT diode, BARITT diode. Parametric Devices & Parametric amplifiers (in brief).	15	CLO2
	Basic principles of light emission in semiconductors, spontaneous		

III	emission, stimulated emission, lasing, lasing threshold, efficiency of light emission. Semiconductor lasers, the laser diode, basic heterostructure, laser structure, SH lasers, DH lasers, Electro-luminescence, LED materials and construction, LED's structures for optical communication applications. Display devices-liquid crystal displays	15	CLO3
IV	Quantum well devices: Quantum well lasers, Quantum well detectors, Integrated Optical detectors, factors limiting performance of integrated detectors. Optical fiber communication-Propagation in Fibers, step index fibers, graded index fibers, multipath dispersion, material dispersion combined effect, Attenuation in optical fibers, Semiconductors PIN photodiode detectors and Avalanche Photodiode Detectors for optical communication application, Optical fiber communication systems.	15	CLO4
Total Contact Hours		60	

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. Microwave Devices and Circuits by Samuel Y. Liao (Prentice Hall India).
2. Electronic Communication Systems by G. Kennedy (TMH).
3. Microwave Engineering by R. Chatterjee.
4. Microwave Semiconductor Devices and their Circuit Applications by H.A. Watson (McGraw Hill).
5. Integrated Optics: Theory & Technology (3rd edition) by R.G. Hunsperger.
6. Optoelectronics-An Introduction (2nd edition) by J. Wilson, J.F.B. Hawkes.
7. Optical Communication Systems by John Gowar.

Evaluation Method

Outcomes	**Internal Assessment (30 Marks)**			**End Semester Examination (70 Marks)**
	Mid Term Exam	Seminar/Presentation/ Assignment/Quiz/Test	**Class Participation**	**SEE**
Marks:	**15**	**10**	**5**	**70**
CLO1	7.5	-	-	17
CLO2	7.5		-	17
CLO3		5		18
CLO4		5		18

w.e.f. session: 2025-26			
Part A - Introduction			
Name of Programme	M.Sc. Electronic Science		
Semester	Third		
Name of the Course	Custom Microelectronics & ASICs		
Course Code	M24-ELE-303		
Course Type	DEC-1		
Level of the course	500-599		
Pre-requisite for the course	NIL		
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO 1: To differentiate among the different types of approaches to implement circuits on IC CLO 2: To differentiate among the different types of ASICs and the process involved in their implementation. CLO 3: To compare various simulation types and delay models. CLO 4: To understand the various processes involved in chip layout and testing		
Credits	Theory	Practical	Total
	4	0	4
Teaching Hours per week	4	0	4
Internal Assessment Marks	30	0	30
End Term Exam Marks	70	0	70
Max. Marks	100	0	100
Examination Time	3 hours		

Part B- Contents of the Course

Instructions for Paper- Setter: The examiner will set 9 questions asking two questions from each unit and one compulsory question by taking course learning outcomes (CLOs) into consideration. The compulsory question (Question No. 1) will consist at least 4 parts covering entire syllabus. The examinee will be required to attempt 5 questions, selecting one question from each unit and the compulsory question. All questions will carry equal marks.

Unit	Topics	Contact Hours	CLOs
I	Microelectronics evolution, why custom microelectronics, Custom microelectronic techniques. Full hand-crafted custom design, fixed cell architectures, soft cell architectures, macrocells, Analog cells, Gate array techniques, sea of gates, Routing considerations.	15	CLO1
II	ASIC design flow, ASIC library design, Programmable ASIC's, ASIC construction, physical design, CAD tools, System partitioning, FPGA partitioning, partitioning methods.	15	CLO2
III	Types of simulation, structural simulation, static timing analysis, Gate level simulation, Net capacitance, Logic systems, cell models, delay models static timing analysis, Formal verification, Switch level simulation, Transistor level simulation.	16	CLO3
IV	Low level design entry, Schematic entry, Floor planning and placement, Floor planning goals and objectives, placement terms and definitions, Goals and objectives physical design flow, **Routing:** global routing, Detailed routing, Special routing, testing, Importance of testing, Boundary Scan test, Faults, Automatic test pattern generation, Built in self-test, Simple test example	14	CLO4
		Total Contact Hours	60

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. Custom VLSI Microelectronics by Stanley L. Hurst (Prentice Hall 1992)
2. Application-Specific Integrated Circuit by Michael John Sebastian Smith (Addison Wesley)
3. Application-Specific Integrated Circuit (ASIC) Technology-Academic Press.

Evaluation Method

Outcomes	**Internal Assessment (30 Marks)**			**End Semester Examination (70 Marks)**
	Mid Term Exam	Seminar/Presentation/ Assignment/Quiz/Test	**Class Participation**	**SEE**
Marks :	**15**	**10**	**5**	**70**
CLO1	5	-	-	15
CLO2	5	2.5	-	20
CLO3	5	2.5		20
CLO4		5		15

w.e.f. Session: 2025-26			
Part A - Introduction			
Name of Programme	M.Sc Electronic Science		
Semester	Third		
Name of the Course	Foundations of MEMS		
Course Code	M24-ELE-304		
Course Type	DEC-1		
Level of the course	500-599		
Pre-requisite for the course (if any)			
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO 1: Ability to understand the multidisciplinary nature, components, need, principle of operation and applications of MEMS CLO 2: Ability to understand various sensing and actuation mechanism used in MEMS devices and compare their merits and demerits. CLO 3: Ability to understand the choice of material and fabrication processes for MEMS CLO 4: Ability to design the MEMS device for specific application and simulate design using MEMS design tools		
Credits	Theory	Practical	Total
	4	0	4
Teaching Hours per week	4	0	4
Internal Assessment Marks	30	0	30
End Term Exam Marks	70	0	70
Max. Marks	100	0	100
Examination Time	3 hours		

Part B- Contents of the Course

Instructions for Paper- Setter: The examiner will set 9 questions asking two questions from each unit and one compulsory question by taking course learning outcomes (CLOs) into consideration. The compulsory question (Question No. 1) will consist at least 4 parts covering entire syllabus. The examinee will be required to attempt 5 questions, selecting one question from each unit and the compulsory question. All questions will carry equal marks.

Unit	Topics	Contact Hours	CLOs
I	**MEMS & Microsystem**- Definition, Typical MEMS and Microsystems Products Microsystems vs MEMS, Microsystems vs Microelectronics, Multidisciplinary nature of Microsystem design and Manufacture, Why miniaturization? Intergrated Microsystems :- Micromechanical Structures, Microsensors, Microactuators , Applications of MEMS and Microsystems **Sensors and Actuator**s :Energy Domains and Transducers, Sensor Consideration, Actuator Considerations, Scaling in MEMS (Ref-2)	15	CLO1
II	**Scaling laws in Miniaturisation** :Scaling in Geometery, Rigid Body Dynamics, Electrostatics forces, Magnetostatic Forces, Fluid Mechanics, Heat transfer, Diffusion and Electricity **Working principles of MEMS :** **Microsensors :**Pressure sensor, Thermal sensors**,** Optical Sensors, Chemical Sensors, Biosensors, Acoustic Wave Sensors **Microactuation :** Actuation using thermal forces, piezoelectric	15	CLO2

	crystals, Shape Memory Alloys and Electrostatic forces **Microactuators** : Microgripper, micromotor, microvalves and micropumps Micro-accelerometer and microfluidics		
III	**Micromachining Technologies :** Microfabrication and Material for MEMS : Si as substrate material, mechanical properties of Silicon, Silicon Compounds (SiO_2, Si_3N_4, SiC, polySi, Silicon), Piezoresistors, Piezoelectric crystals, Polymers, Packaging Materials. Micromachining Processes: Overview of microelectronic fabrication processes used in MEMS, Bulk Micromachining, Anisotropic wet etching, DRIE, Etch stop techniques, Surface Micromachining – General description, Case studies using MEMS Design Tools	15	CLO3
IV	**Intergration of Micro and Smart Systems** **Intergartion of Microsystems and Microelectronics** : CMOS First, MEMS First, Other Integration Approaches **Microsystems Packaging :**Objectives of Packaging, Special issues in Microsystems Packaging , Types of Microsystem Packaging , Packaging technology, Case study of Pressure Sensor and Micromachined Accelerometer as Integrated Microsystems . Case study of PZT Transducer and Vibrations in Beam as a smart structure in Vibration Control	15	CLO4
	Total Contact Hours	60	

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. Foundations of MEMS, Liu, Pearson India
2. Microfabrication by Marc Madao, CRC Press
3. MEMS & Microsystems Design and Manufacture by Tai-Ran H Su, Tata Mcgraw
4. Microsystem Design by S.D. Senturia, Ruiwer Academic Publisher
5. Micro and Smart Systems by Anathasuresh et. Al. , Wiley India

Evaluation Method

Outcomes	**Internal Assessment (30 Marks)**			**End Semester Examination (70 Marks)**
	Mid Term Exam	Seminar/Presentation/ Assignment/Quiz/Test	**Class Participation**	**SEE**
Marks:	**15**	**10**	**5**	**70**
CLO1	5	2.5	-	17
CLO2	5	2.5	-	17
CLO3	2.5	2.5		18
CLO4	2.5	2.5		18

w.e.f. Session: 2025-26			
Part A - Introduction			
Name of Programme	M.Sc. Electronic Science		
Semester	Third		
Name of the Course	Advanced Semiconductor Manufacturing		
Course Code	M24-ELE-305		
Course Type	DEC-1		
Level of the course	500-599		
Pre-requisite for the course	M24-ELE-102: IC Fabrication Technology		
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO 1 : Understand the role of various materials used in VLSI fabrication technology CLO 2 : Understand various mechanism of the process technology for physical implementation of different materials in IC Fabrication CLO 3 : Analyze the choice of material and fabrication processes for IC Fabrication CLO 4: Skill to conduct research on new materials for VLSI and able to work in IC fabrication laboratory.		
Credits	Theory	Practical	Total
	4	0	4
Teaching Hours per week	4	0	4
Internal Assessment Marks	30	0	30
End Term Exam Marks	70	0	70
Max. Marks	100	0	100
Examination Time	3 hours		

Part B- Contents of the Course

Instructions for Paper- Setter: The examiner will set 9 questions asking two questions from each unit and one compulsory question by taking course learning outcomes (CLOs) into consideration. The compulsory question (Question No. 1) will consist at least 4 parts covering entire syllabus. The examinee will be required to attempt 5 questions, selecting one question from each unit and the compulsory question. All questions will carry equal marks.

Unit	Topics	Contact Hours	CLOs
I	Wafer shaping process cleaning mechanical properties of the wafer, Silicon wafer criteria for VLSI/ULSI technology, High technology silicon wafer concept, VLSI/ULSI wafer characteristics, structural and chemical and mechanical characteristics.	15	CLO1
II	Silicon nitride, nitride properties of silicon nitride, plasma-assisted deposition, deposition variable, properties of plasma assisted deposited filing, other material, stability and semiconductor and insulating, patterning, Self-aligned silicides.	15	CLO2
III	materials for contacts and interconnects, Metallization, Applications, gates and interconnections, Ohmic contacts, Metallization choices, Metals or allays properties, Metallization problem, metallurgical and chemical interactions, electro-migration, new role of metallization, multilevel structures, epitaxial metals, diffusion barriers and redundant metal links	16	CLO3
IV	Assembly and packaging of VLSI devices package types, packaging design considerations, thermal design considerations, electrical considerations, mechanical design considerations, VLSI assembly technologies, wafer preparation, die-banding, wire bonding, package fabrication technologies ceramic package, glass-sealed refractory package, plastic molding	14	CLO4

	technology molding process, special package considerations.		
		Total Contact Hours	60

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. Semiconductor Silicon Crystal Technology, Fumio Shimura, academic Press, Inc.
2. VLSI Technology, SM Sze, McGraw Hill International Ed.

Evaluation Method

Outcomes	**Internal Assessment (30 Marks)**			**End Semester Examination (70 Marks)**
	Mid Term Exam	Seminar/Presentation/ Assignment/Quiz/Test	**Class Participation**	**SEE**
Marks :	**15**	**10**	**5**	**70**
CLO1	5	-	-	15
CLO2	5	2.5	-	20
CLO3	5	2.5		20
CLO4		5		15

w.e.f. session: 2025-26			
Part A - Introduction			
Name of Programme	M.Sc Electronic Science		
Semester	Third		
Name of the Course	Digital Communication		
Course Code	M24-ELE-306		
Course Type	DEC-1		
Level of the course	500-599		
Pre-requisite for the course (if any)	Student should be well versed with Fourier Series, Fourier Transforms, Probability Theory		
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO 1: Ability to understand need and applications of the Digital Communication CLO 2: Ability to Understand the design and performance parameters of component blocks CLO 3: Ability to understand various digital modulation and error correction techniques CLO 4: Ability to Understand the digital transmission of Analog signals		
Credits	Theory	Practical	Total
	4	0	4
Teaching Hours per week	4	0	4
Internal Assessment Marks	30	0	30
End Term Exam Marks	70	0	70
Max. Marks	100	0	100
Examination Time	3 hours		

Part B- Contents of the Course

Instructions for Paper- Setter: The examiner will set 9 questions asking two questions from each unit and one compulsory question by taking course learning outcomes (CLOs) into consideration. The compulsory question (Question No. 1) will consist at least 4 parts covering entire syllabus. The examinee will be required to attempt 5 questions, selecting one question from each unit and the compulsory question. All questions will carry equal marks.

Unit	Topics	Contact Hours	CLOs
I	**Unit I** Introduction: Model of Communication System, Elements of a Digital Communication System, Analysis and Design of Communication System, Classification of Signals and Systems A brief review of Random Signal Theory : Probabilities, Random Variables and Random Processes Information and Channel Capacity : Measure of Information, Encoding of the Source output – Shannon Encoding Algorithm and Huffman Encoding algorithm (Ref. 3), Discrete Communication Channels : Only Memoryless, Continuous Communication Channel : Shannon- Hartley Theorem	15	CLO1 CLO2
II	Digital Modulation Techniques: Introduction, Binay Phase-Shift Keying, Differential Phase-Shift Keying, Differentially- Encoded PSK, Quardrature Phase Shift Keying, M-ary PSK, Quadrature Amplitude Shift Keying, Binary FSK, Similarity of BFSK and BPSK, M-ary FSK, Minimum Shift Keying, Duobinary Encoding, A Comparison of Narrowband FM System (Ref 2)	15	CLO3 CLO3
III	Error control coding : Examples of Error control coding, Methods of controlling errors, Types of errors and codes, Linear block codes,	15	CLO3 CLO4

	Binary cyclic codes. Convolutional Codes-Trellis Code		
IV	Digital Transmission of Analog Signals, Sampling theory and Practice, Quantizing of Analog Signals, , PCM, Delta Modulation, Q-level differential PCM, Time Division Multiplexing, Spread Spectrum and Multiple Access Techniques, Introduction to Spread Spectrum Modulation , Code Acquisition and Tracking , Spread Spectrum as a Multiple Access Techniques.	15	CLO4
	Total Contact Hours	60	

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. Digital and Analog Communication Systems by K. Sam Shanmugan (John wiley & Sons 1994).
2. Principles of Communication System by Taub and Schilling (McGraw Hill International).
3. An Introduction to Analog & Digital Communication by Simon Haykin.
4. John G.Proakis, "Digital Communication" McGraw Hill 3rd Edition, 1995

Evaluation Method

Outcomes	**Internal Assessment (30 Marks)**			**End Semester Examination (70 Marks)**
	Mid Term Exam	Seminar/Presentation/ Assignment/Quiz/Test	**Class Participation**	**SEE**
Marks:	**15**	**10**	**5**	**70**
CLO1	5	2.5	-	17
CLO2	5	2.5	-	17
CLO3	2.5	2.5		18
CLO4	2.5	2.5		18

w.e.f. session: 2025-26			
Part A - Introduction			
Name of Programme	M.Sc Electronic Science		
Semester	Third		
Name of the Course	Advanced Embedded Systems		
Course Code	M24-ELE-307		
Course Type	DEC-2		
Level of the course	500-599		
Pre-requisite for the course (if any)			
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO 1: Ability to understand need and applications of 32-bit Embedded Systems CLO 2: Ability to analyze given problem and write programs using ARM assembly and C language CLO 3: Ability to design interfacing circuits using standard peripherals CLO 4: Ability to understand the need and applications of DSP Procesors		
Credits	Theory	Practical	Total
	4	0	4
Teaching Hours per week	4	0	4
Internal Assessment Marks	30	0	30
End Term Exam Marks	70	0	70
Max. Marks	100	0	100
Examination Time	3 hours		

Part B- Contents of the Course

Instructions for Paper- Setter: The examiner will set 9 questions asking two questions from each unit and one compulsory question by taking course learning outcomes (CLOs) into consideration. The compulsory question (Question No. 1) will consist at least 4 parts covering entire syllabus. The examinee will be required to attempt 5 questions, selecting one question from each unit and the compulsory question. All questions will carry equal marks.

Unit	Topics	Contact Hours	CLOs
I	**32-Bit or Higher Order Processors** **Intel 80386DX :** Architecture , Interrupt Facilities, Instruction Set , 80387 floating point co-processor **INTEL 80486 :**Instruction set **Intel 486SX and overdrive processors Intel Pentium :** Multiple branch prediction , Data flow analysis Speculative Execution, The MMX instructions Pentium-II **Integrated Processors** **RISC processors :**: **The Berkeley RISC model ,Sun SPARC RISC processor Architecture** Interupts, instruction set, The stanford RISC Model **The MPC603 block diagram** **The ARM**: register set , Exceptions , The Thumb instructions **Digital signal processors, DSP Basic Architecture, Chossing a Processor**	14	CLO1
II	**ARM : Architecture and Assembly Language Programming** Architecture, Interrupt Vector Table, Programming the ARM Proces-sors ARM Assembly Language , ARM Instruction Set , Conditional Exe-	16	CLO2

	cution Arithmetic Instructions , Logical Instructions , Compare Instructions Multiplication, Division		
III	Starting Assembly Langauge Program General Structure of an Assembly Language, Writing Assembly Programs , Branch Instructions , Loading Constants ,Load and Store Instructions ,Readonly and Read/Write Memory,Multiple Register Load and Store **ARM :Peripheral Programming of ARM MCU using C** Block Diagram , Features of the LPC 214x Family Peripherals ARM 9 ,ARM Cortex-M3	16	CLO2 CLO3
IV	**DSP Processors** The Application Scenario ,General Features of Digital Signal Processors SIMD Techniques ,The SHARC Floating Point Processor ,DSP Processors of Texas Instruments (TI) ,OMAP (Open Multimedia Applications Platform	14	CLO4
	Total Contact Hours	60	

Suggested Evaluation Methods			
Internal Assessment: 30		**End Term Examination: 70**	
Theory	**30**	**Theory**	**70**
• Class Participation:	5	Written Examination	
• Seminar/Presentation/Assignment/Quiz/Class test etc.:	10		
• Mid-Term Exam:	15		

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. Embedded Systems-An integrated Approach , Layla B. Das, 1st edition Pearson, 2012
2. Embedded System Design, Steve Heath, 2nd Edition, Elsevier , 2005
3. Introduction to Embedded Systems : Shibu K. V. (TMH

Evaluation Method

Outcomes	**Internal Assessment (30 Marks)**			**End Semester Examination (70 Marks)**
	Mid Term Exam	Seminar/Presentation/ Assignment/Quiz/Test	**Class Participation**	**SEE**
Marks:	**15**	**10**	**5**	**70**
CLO1	7.5	-	-	17
CLO2	7.5		-	17
CLO3		5		18
CLO4		5		18

w.e.f. Session: 2025-26			
Part A - Introduction			
Name of Programme	M.Sc. Electronic Science		
Semester	Third		
Name of the Course	Chip Implementation with Physical Design		
Course Code	M24-ELE-308		
Course Type	DEC-2		
Level of the course	500-599		
Pre-requisite for the course	Knowledge of MOS Devices & IC Fabrication process		
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO 1 : Analysis the different types of RAM, ROM designs. CLO 2 : To study about architecture and operations of different semiconductor memories CLO 3 : Analysis of different memory testing and design for testability CLO 4: Identification of new developments in semiconductor memory design.		
Credits	Theory	Practical	Total
	4	0	4
Teaching Hours per week	4	0	4
Internal Assessment Marks	30	0	30
End Term Exam Marks	70	0	70
Max. Marks	100	0	100
Examination Time	3 hours		

Part B- Contents of the Course

Instructions for Paper- Setter: The examiner will set 9 questions asking two questions from each unit and one compulsory question by taking course learning outcomes (CLOs) into consideration. The compulsory question (Question No. 1) will consist at least 4 parts covering entire syllabus. The examinee will be required to attempt 5 questions, selecting one question from each unit and the compulsory question. All questions will carry equal marks.

Unit	Topics	Contact Hours	CLOs
I	Introduction to Physical Design and EDA Tools: Introduction to Physical Design SoC Flow. Overview of the complete Physical Design SoC flow. Introduction to EDA Tools. Overview of Synopsys, Cadence, Siemens, and open-source alternatives. Standard Cell and Key Design Elements. Analysis of standard cells and essential design elements. Hands-on exercises using EDA tools.	15	CLO1
II	Logic & Physical Synthesis and Timing Analysis Logic & Physical Synthesis Application of logic synthesis techniques. Physical synthesis for placement and routing optimization. Timing Constraints and Analysis. Definition and implementation of timing constraints. Analysis of timing characteristics and mitigation strategies.	15	CLO2
III	Floor Planning, Placement, and Clock Tree Synthesis: Floor Planning and Placement. Development of floor plans for efficient chip layout. Optimization of chip placement for performance and area. Clock Tree Synthesis and Routing. Implementation of clock tree synthesis. Routing techniques for interconnections within the design.	16	CLO3
IV	Timing Closure, Physical Design Verification, and Tape-Out: Timing Closure Techniques. Application of techniques to achieve timing closure. Addressing challenges in meeting timing requirements. Physical	14	CLO4

	Design Verification, Tape-Out, and DFT/DFM Introduction: Methods for physical design verification. Overview of the tape-out process. Introduction to Design for Testability (DFT) and Design for Manufacturability (DFM) principles.		
		Total Contact Hours	60

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. Cem Unsalan, Bora Tar. Digital System Design with FPGA: Implementation using Verilog and VHDL. McGraw-Hill, First Edition.
2. Nekoogar, Farzad. From ASICs to SOCs. Prentice Hall Professional, 2003.
3. Chakravarthi, Veena. SoC Physical Design. Springer Nature, 2022.
4. Kahng, Andrew. VLSI Physical Design: From Graph Partitioning to Timing Closure. Springer Science & Business Media, 2011.
5. Michael Keating, Synopsys. The Simple Art of SoC Design. Springer Science & Business Media, 2011.
6. Sait, Sadiq. VLSI Physical Design Automation. World Scientific, 1999.

Evaluation Method

Outcomes	**Internal Assessment (30 Marks)**			**End Semester Examination (70 Marks)**
	Mid Term Exam	Seminar/Presentation/ Assignment/Quiz/Test	**Class Participation**	**SEE**
Marks :	**15**	**10**	**5**	**70**
CLO1	5	-	-	15
CLO2	5	2.5	-	20
CLO3	5	2.5		20
CLO4		5		15

w.e.f. Session: 2025-26			
Part A - Introduction			
Name of Programme	M.Sc. Electronic Science		
Semester	Third		
Name of the Course	Nanoelectronics: Nano-CMOS & beyond		
Course Code	M24-ELE-309		
Course Type	DEC-2		
Level of the course	500-599		
Pre-requisite for the course	MOS Devices and CMOS Circuits		
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO 1 : Understand various issues related to nanoscale electronic devices. CLO 2 : Compare various techniques for creating low dimensional semiconductor nanostructures CLO 3 : Synthesize nanostructures/devices for electronics applications CLO 4: Explain the techniques used for characterization of nano electronic structures.		
Credits	Theory	Practical	Total
	4	0	4
Teaching Hours per week	4	0	4
Internal Assessment Marks	30	0	30
End Term Exam Marks	70	0	70
Max. Marks	100	0	100
Examination Time	3 hours		

Part B- Contents of the Course

Instructions for Paper- Setter: The examiner will set 9 questions asking two questions from each unit and one compulsory question by taking course learning outcomes (CLOs) into consideration. The compulsory question (Question No. 1) will consist at least 4 parts covering entire syllabus. The examinee will be required to attempt 5 questions, selecting one question from each unit and the compulsory question. All questions will carry equal marks.

Unit	Topics	Contact Hours	CLOs
I	Overview of progress of microelectronics worldwide. International technology roadmap characteristics. Short channel MOS devices, CMOS scaling types; Constant field scaling, constant voltage scaling. Nanoscale MOSFET, FinFET, vertical MOSFETS's limits of CMOS technology. Materials & processes for advanced sub 65nm CMOD technology.	15	CLO1
II	From microelectronics towards nanoelectronics. Noval approaches towards future devices. Introduction to nanotechnology and nanomaterials. Applications in different fields. Bottom up and top-down approaches	15	CLO2
III	Semiconductor Low dimensional systems- Two dimensional confinement of carriers, Quantum wells, One dimensional Quantum systems; quantum wires, Zero dimensional quantum structures: Quantum Dots.	16	CLO3
IV	Quantum devices: Resonant tunneling diode & transistor. Coulomb Blockade, Single Electron Transistor, Introduction to Spintronics, Material requirements for spintronics, Spin devices: Spin Transistor, Spin values etc.	14	CLO4
	Total Contact Hours	60	

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. Semicond"Nanoelectronics and Information Technology", (Advanced Electronic and Novel Devices), Waser Ranier, Wiley- VCH (2003)

2. “The Physics of Low-dimensional Semiconductors”. John H. Davies, Cambridge University Press, 1998.
3. “Introduction to Nano Technology”, John Wiley & Sons, 2003.
4. “Introduction to Molecular Electronics”, M.C. Petty, M.R.Bryce, and D.Bloor, Edward Arnold (1995).
5. “Quantum Hetrostructures”, V.Mitin, V. Kochelap, and M.Stroscio, Cambridge University Press.

Evaluation Method

Outcomes	**Internal Assessment (30 Marks)**			**End Semester Examination (70 Marks)**
	Mid Term Exam	Seminar/Presentation/ Assignment/Quiz/Test	**Class Participation**	**SEE**
Marks :	**15**	**10**	**5**	**70**
CLO1	5	-	-	15
CLO2	5	2.5	-	20
CLO3	5	2.5		20
CLO4		5		15

w.e.f. Session: 2025-26			
Part A - Introduction			
Name of Programme	M.Sc. Electronic Science		
Semester	Third		
Name of the Course	Emerging Memory Devices		
Course Code	M24-ELE-310		
Course Type	DEC-2		
Level of the course	500-599		
Pre-requisite for the course	NIL		
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO 1 : Analysis the different types of RAM, ROM designs. CLO 2 : To study about architecture and operations of different semiconductor memories CLO 3 : Analysis of different memory testing and design for testability CLO 4: Identification of new developments in semiconductor memory design.		
Credits	Theory	Practical	Total
	4	0	4
Teaching Hours per week	4	0	4
Internal Assessment Marks	30	0	30
End Term Exam Marks	70	0	70
Max. Marks	100	0	100
Examination Time	3 hours		

Part B- Contents of the Course

Instructions for Paper- Setter: The examiner will set 9 questions asking two questions from each unit and one compulsory question by taking course learning outcomes (CLOs) into consideration. The compulsory question (Question No. 1) will consist at least 4 parts covering entire syllabus. The examinee will be required to attempt 5 questions, selecting one question from each unit and the compulsory question. All questions will carry equal marks.

Unit	Topics	Contact Hours	CLOs
I	classification of memories **Volatile Memories-1** Static Random Access Memories (SRAMs): SRAM functionality: architecture, timing diagrams, performance and timing specifications; SOI SRAMs; SRAM cell structure- MOS SRAM architecture, MOS SRAM cell and peripheral circuit operation, bipolar SRAM technologies, silicon on insulator (SOI) SRAM, advanced SRAM architectures and technologies, application specific SRAMs	15	CLO1
II	**Volatile Memories-2** Dynamic Random Access Memories (DRAMs): DRAM technology development, CMOS CRAMs, 3-transistor DRAM; 1 transistor DRAM: functionality, architecture, timing diagrams, performance and timing specifications; sense amplifier; word line driver; leakage mechanisms in a DRAM; retention; retention time calculations.	15	CLO2
III	**Nonvolatile Memories** FLASH memories; floating gate theory; structure and working of a SONOS cell; structure and working FLOTOX memories; multi-level flash memories; NOR based flash memories; NAND based flash memories. **Non-silicon based Memories**	16	CLO3

	PCRAM; Resistive RAM (RRAM), FeRAM; array device considerations for non-silicon based memories, Gallium Arsenide (GaAs) FRAMs, Analog memories: magnetoresistive random access memories (MRAMs), Experimental memory devices.		
IV	Nonvolatile Memories: Masked Read, only memories (ROMs): High density ROMs, programmable read-only memories (PROMs)- bipolar PROMs, CMOS PROMs, erasable (UV)- Programmble read-only memories (EPROMs)- Floating Gate EPROM cell- one, time progammable (OTP) Eproms Electrically Erasable PROMs (EEPROMs), EEPROM technology and architecture, nonvolatile SRAM-Flash memories (EPROMs or EEPROM), Advanced flash memory architecture	14	CLO4
		Total Contact Hours	60

Part C-Learning Resources

Recommended Books/e-resources/LMS:

7. Ashok K.Sharma, Semiconductor Memories Technology, testing and reliability, Prentice hall of India Private Limited, New Delhi 1997.
8. Ashok K Sharna, Advanced Semiconductor Memories – Architecture, Design and Applications, Wiley 2002.
9. Anjan Ghosh, High Speed Semiconductor Devices, NPTEL Courseware, 2009.
10. W. D. Brown, and Joe Brewer, Nonvolatile Semiconductor Memory Technology: A Comprehensive Guide to Understanding and Using NVSM Devices, WileyIEEE Press, 1997.
11. J. Brewer, Nonvolatile Memory Technologies with Emphasis on Flash: A Comprehensive Guide to Understanding and Using Flash Memory Devices, Manzur Gill, Wiley-IEEE Press, 2008.

Evaluation Method

Outcomes	**Internal Assessment (30 Marks)**			**End Semester Examination (70 Marks)**
	Mid Term Exam	Seminar/Presentation/ Assignment/Quiz/Test	**Class Participation**	**SEE**
Marks :	**15**	**10**	**5**	**70**
CLO1	5	-	-	15
CLO2	5	2.5	-	20
CLO3	5	2.5		20
CLO4		5		15

w.e.f. Session: 2025-26			
Part A - Introduction			
Name of the Programme	M.Sc Electronic Science		
Semester	Third		
Name of the Course	Electronic Communication Lab		
Course Code	M24-ELE-311		
Course Type	PC-5		
Level of the course	500-599		
Pre-requisite for the course (if any)	NIL		
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO1: Familiarize with Simulation Tools, Test Benches used in designing of communication systems CLO2: Perform the simulation of electronic communication circuits. CLO3: Analyze & Interpret the data obtained in the experiments. CLO4: Present the experimental results and conclusions in the form of written report in clear and concise manner.		
Credits	Theory	Practical	Total
	0	4	4
Teaching Hours per week	0	8	8
Internal Assessment Marks	0	30	30
End Term Exam Marks	0	70	70
Max. Marks	0	100	100
Examination Time	0	4 hours (or as decided by PGBOS)	

Part B- Contents of the Course

Practicals	Contact Hours
This is tentative list of experiments. List may change with every semester as per Cos with approval of chairperson/staff council 1. Digital Communication-PCM using kit & MATLAB/Octave 2. Digital Communication-PWM using kit & MATLAB/Octave 3. Digital Communication-Delta Modulation using kit & MATLAB 4. Digital Communication-PPM using kit & MATLAB 5. MOSCAP fabrication (Cleaning, oxidation and metallization) 6. CV characterization of MOSCAP and extraction of various parameters from CV curve. 7. Microwave applications using Microwave bench	120

Suggested Evaluation Methods

Internal Assessment: 30		End Term Examination: 70	
➢ **Practicum**	**30**	➢ **Practicum**	**70**
• Class Participation:	5	Lab record, Viva-Voce, write-up and execution of the practical	
• Seminar/Demonstration/Viva-voce/Lab records etc.:	10		
• Mid-Term Exam:	15		

Part C-Learning Resources

Recommended Books/e-resources/LMS:

- Lab Manual of respective experiments

w.e.f. Session: 2025-26			
Part A - Introduction			
Name of the Programme	M.Sc Electronic Science		
Semester	Third		
Name of the Course	EDA Tools for design & simulation		
Course Code	M24-ELE-312		
Course Type	PC-6		
Level of the course	500-599		
Pre-requisite for the course (if any)	NIL		
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO1: Operate various CAD tools for designing and simulation of electronic systems CLO2: Write and execute the programs for embedded systems CLO3: Analyze & Interpret the data obtained in the experiments CLO4: Present the experimental results and conclusions in the form of written report in clear and concise manner		
Credits	Theory	Practical	Total
	0	4	4
Teaching Hours per week	0	8	8
Internal Assessment Marks	0	30	30
End Term Exam Marks	0	70	70
Max. Marks	0	100	100
Examination Time	0	4 hours (or as decided by PGBOS)	

Part B- Contents of the Course

practicals	Contact Hours
This is tentative list of experiments. List may change with every semester as per Cos with approval of chairperson/staff council **Section-A CAD Tools** 1. VHDL/Verilog based behavioural design. 2. VHDL/Verilog based dataflow. 3. VHDL/Verilog Architectural design of digital circuits. 4. Synthesis of a digital circuit a demonstrating its working on FPGA / CPLD. 5. Device/Process simulation using Silvaco/open source simulator. 6. CMOS Inverter Design using Cadence/Backend **Section-B** 1. a) Study of LPC2148 Microcontroller Architecture. b) Familiarization with Tool. c) Debug Practice with LPC2148 Kit d) Write simple programs in Embedded C for LPC 2148. 2. Sine wave generation using microcontroller 3. Resistive (PT100) temp sensor interface with microcontroller.	120

Suggested Evaluation Methods

Internal Assessment: 30		End Term Examination: 70	
➢ **Practicum**	**30**	➢ **Practicum**	**70**
• Class Participation:	5	Lab record, Viva-Voce, write-up and execution of the practical	
• Seminar/Demonstration/Viva-voce/Lab records etc.:	10		
• Mid-Term Exam:	15		

Part C-Learning Resources

Recommended Books/e-resources/LMS:

- Lab manuals of respective experiments

w.e.f. Session: 2025-26			
Part A - Introduction			
Name of Programme	M.Sc. Electronic Science		
Semester	Fourth		
Name of the Course	VHDL for Digital Design		
Course Code	M24-ELE-401		
Course Type	DEC-3		
Level of the course	500-599		
Pre-requisite for the course	Digital circuits & system Design & Verilog Hardware Description Language		
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO 1: Describe the basic concepts of VHDL language CLO 2: Classify behavior level modeling CLO 3: Demonstrate data flow level modeling and Structural modeling CLO 4: Demonstrate the combinational & sequential circuits using VHDL		
Credits	Theory	Practical	Total
	4	0	4
Teaching Hours per week	4	0	4
Internal Assessment Marks	30	0	30
End Term Exam Marks	70	0	70
Max. Marks	100	0	100
Examination Time	3 hours		

Part B- Contents of the Course

Instructions for Paper- Setter: The examiner will set 9 questions asking two questions from each unit and one compulsory question by taking course learning outcomes (CLOs) into consideration. The compulsory question (Question No. 1) will consist at least 4 parts covering entire syllabus. The examinee will be required to attempt 5 questions, selecting one question from each unit and the compulsory question. All questions will carry equal marks.

Unit	Topics	Contact Hours	CLOs
I	**Introduction to VHDL** Basic Terminology, Entity declaration,Architectural Body, Configuration Declaration, Package Declaration, Package Body, Identifiers, Data Objects, Data Types, Operators	15	CLO1
II	**Behavioral Modeling Process** Statement,Variable Assignment Statement,Signal Assignment Statement,wait statement, if statement, case statement, null statement, loop statement, next statement, Assertion statement, Delay models, Other Sequential Statements, multiple process statement,Simulation:Writing a Test bench.	15	CLO2
III	**Dataflow Modeling** Concurrent Signal Assignment, Concurrent versus sequential signal Assignment Statement,Conditional Signal Assignment statement, selected signal assignment statement. Structural Modeling: Component Declaration, Component Instantiation, Examples	16	CLO3
IV	**Combinational Logic design using VHDL** Decoders, encoders, priority encoder, multiplexers and demultiplexers, Code Converters, Parity circuits, comparators, Adders & subtractors, ALUs. **Sequential Logic design using VHDL** Latches and flip-flops, counters, shift registers, Modeling Moore FSM, Modeling Mealy FSM Design.	14	CLO4
	Total Contact Hours	60	

Part C-Learning Resources
Recommended Books/e-resources/LMS: 1. J.Bhasker, "VHDL Primer", Pearson Education/PHI, 2015 2. John F.Wakerly, "Digital Design Principles & Practices", PHI/Pearson Education Asia, 3rd Ed., 2005.

Evaluation Method

Outcomes	Internal Assessment (30 Marks)			End Semester Examination (70 Marks)
	Mid Term Exam	Seminar/Presentation/ Assignment/Quiz/Test	**Class Participation**	**SEE**
Marks :	**15**	**10**	**5**	**70**
CLO1	5	-	-	15
CLO2	5	2.5	-	20
CLO3	5	2.5		20
CLO4		5		15

Session: 2025-26			
Part A - Introduction			
Name of Programme	M.Sc Electronic Science		
Semester	Fourth		
Name of the Course	System Verilog		
Course Code	M24-ELE-402		
Course Type	DEC-3		
Level of the course	500-599		
Pre-requisite for the course (if any)	Digital Design, Verilog		
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO 1:Ability to understand need and applications of SystemVerilog CLO 2:Ability to Understand the syntax of System Verilog CLO 3:Ability to understand different design methods using SystemVerilog CLO 4: Ability to design complex systems using SystemVerilog		
Credits	Theory	Practical	Total
	4	0	4
Teaching Hours per week	4	0	4
Internal Assessment Marks	30	0	30
End Term Exam Marks	70	0	70
Max. Marks	100	0	100
Examination Time	3 hours		

Part B- Contents of the Course

Instructions for Paper- Setter: The examiner will set 9 questions asking two questions from each unit and one compulsory question by taking course learning outcomes (CLOs) into consideration. The compulsory question (Question No. 1) will consist at least 4 parts covering entire syllabus. The examinee will be required to attempt 5 questions, selecting one question from each unit and the compulsory question. All questions will carry equal marks.

Unit	Topics	Contact Hours	CLOs
I	**An introduction to gate-Level Design Using System Verilog** Important rules for using an HDL, Lvels of Design Abstraction, Basic Structural System Verilog Design, Declaring wires in system Verilog, CAD tool design flow. Creating hierarchy via structural Instantiation, specifying constants in system Verilog, accessing bits of multi-bit wire, naming modules, wiresand instance names, hierarchial design flow	15	CLO1
II	**Dataflow SystemVerilog** A Basic 2:1 MUX , Dataflow Operators , a 2:4 Decoder , Parameterization in Dataflow SystemVerilog, SystemVerilog and Arithmetic . **Behavioral SystemVerilog for Registers** Introduction to Behavioral SystemVerilog , The always ff Block, Shift Register Design Using Behavioral SystemVerilog , The Semantics of the always ff Block,Reset Problems With Registers	15	CLO2
III	**Behavioral SystemVerilog for Combinational Logic** Combinational always Blocks The Use of case Statements in always comb Blocks , The Problem With Latches in always comb Blocks , Avoiding Latches When Using case Statements , Mapping SystemVerilog Programs to a Specific Technology **State Machine Design Using SystemVerilog**	15	CLO3

	SystemVerilog Features for Coding State ,The 2-Always Block State Machine Coding ,Enumerated Types for Symbolic State Names ,The always comb IFL/OFL Block ,State Machine Coding Styles .		
IV	**Case Study: A Soda Machine Controller** Understand the Complete System Requirements and Organization, Determine a System Architecture , **Design the System Parts** - Design of the Timer Subsystem , Design of the Keypad Interface Subsystem ,Design of the Central Control Subsystem ,Design of the , Design of the Central Control Subsystem State Machine , A Complete and Conflict-Free State , Implementing the State Machine Using SystemVerilog ,Asynchronous Inputs and Glitch-Free Outputs **Case Study : Design of UART** UART protocol design, Designing UART, Design of UART Transmitter and Receiver SystemVerilog design for bus structure, SystemVerilog vs Verilog	15	CLO4
	Total Contact Hours	60	

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1.“Designing Digital Systems With SystemVerilog” by Dr. Brent E. Nelson,(2018), Independently Published

2. “SystemVerilog for Design Second Edition: A Guide to Using SystemVerilog for Hardware Design and Modeling” by Stuart Sutherland ,Simon Davidmann ,Peter Flake , (2006), Springer-Verlag New York Inc

3. “Introduction to SystemVerilog” by Ashok K. Mehta, (2021), Springer Nature Switzerland AG

Evaluation Method

Outcomes	**Internal Assessment (30 Marks)**			**End Semester Examination (70 Marks)**
	Mid Term Exam	Seminar/Presentation/ Assignment/Quiz/Test	**Class Participation**	**SEE**
Marks:	**15**	**10**	**5**	**70**
CLO1	5	2.5	-	17
CLO2	5	2.5	-	17
CLO3	2.5	2.5		18
CLO4	2.5	2.5		18

w.e.f. Session: 2025-26			
Part A - Introduction			
Name of Programme	M.Sc. Electronic Science		
Semester	Fourth		
Name of the Course	Design for Testability		
Course Code	M24-ELE-403		
Course Type	DEC-3		
Level of the course	500-599		
Pre-requisite for the course	Digital circuits & system Design & Verilog Hardware Description Language		
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO 1 : understand the fundamentals of Design for Testability CLO 2 : know the Scan-Based Testing and Fault Analysis CLO 3 : learn the Strategies and Standards in Testability CLO 4: understand the Emerging trends in DFT		
Credits	Theory	Practical	Total
	4	0	4
Teaching Hours per week	4	0	4
Internal Assessment Marks	30	0	30
End Term Exam Marks	70	0	70
Max. Marks	100	0	100
Examination Time	3 hours		

Part B- Contents of the Course

Instructions for Paper- Setter: The examiner will set 9 questions asking two questions from each unit and one compulsory question by taking course learning outcomes (CLOs) into consideration. The compulsory question (Question No. 1) will consist at least 4 parts covering entire syllabus. The examinee will be required to attempt 5 questions, selecting one question from each unit and the compulsory question. All questions will carry equal marks.

Unit	Topics	Contact Hours	CLOs
I	**Introduction to Design for Testability**: Importance in modern electronic systems, Historical background and evolution, Key concepts: Fault models, testing methodologies, and standards **Built-In Self-Test (BIST) Techniques:** Principles and architecture of BIST, Benefits and limitations, BIST simulations and practical exercises	15	CLO1
II	**Scan-Based Testing and Fault Analysis :** Scan Chains and Serial Testing: Design and use of scan chains, Optimization techniques for better coverage, Design and test of scan chains **Fault Modeling and Simulation:** Types of faults (stuck-at, bridging, etc.), Simulation tools and fault coverage analysis, Fault simulation exercises using CAD tools	15	CLO2
III	**Design for Testability (DFT) Strategies:** Techniques for enhancing testability, Real-world case studies and successful implementations, DFT-aware circuit design and testing Industry **Standards in Testability:** Overview of IEEE standards (e.g., 1149.1 JTAG), Compliance, certification, and validation processes, Testing for standard compliance	16	CLO3
IV	**Advanced Topics in DFT:** Emerging trends in DFT (e.g., AI in testing, low-power DFT), Future challenges and opportunities	14	CLO4
		Total Contact Hours	60

Part C-Learning Resources
Recommended Books/e-resources/LMS: 12. Tripathi, Suman. Advanced VLSI Design and Testability Issues. CRC Press, 2020. 13. Wang, Laung-Terng. VLSI Test Principles and Architectures. Morgan Kaufmann, 2006. 14. Huhn, Sebastian. Design for Testability, Debug and Reliability. Springer Nature, 2021.

Evaluation Method

Outcomes	**Internal Assessment (30 Marks)**			**End Semester Examination (70 Marks)**
	Mid Term Exam	Seminar/Presentation/ Assignment/Quiz/Test	**Class Participation**	**SEE**
Marks :	**15**	**10**	**5**	**70**
CLO1	5	-	-	15
CLO2	5	2.5	-	20
CLO3	5	2.5		20
CLO4		5		15

w.e.f. session: 2025-26			
Part A - Introduction			
Name of Programme	M.Sc Electronic Science		
Semester	Fourth		
Name of the Course	Programming for Electronics using Python		
Course Code	M24-ELE-404		
Course Type	DEC-3		
Level of the course	500-599		
Pre-requisite for the course (if any)	NIL		
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO 1: Ability to understand need and applications of Python CLO 2: Ability to Understand the syntax of Python CLO 3: Ability use python to generate plots CLO 4: Ability to write program in python to simulate a design		
Credits	Theory	Practical	Total
	4	0	4
Teaching Hours per week	4	0	4
Internal Assessment Marks	30	0	30
End Term Exam Marks	70	0	70
Max. Marks	100	0	100
Examination Time	3 hours		

Part B- Contents of the Course

Instructions for Paper- Setter: The examiner will set 9 questions asking two questions from each unit and one compulsory question by taking course learning outcomes (CLOs) into consideration. The compulsory question (Question No. 1) will consist at least 4 parts covering entire syllabus. The examinee will be required to attempt 5 questions, selecting one question from each unit and the compulsory question. All questions will carry equal marks.

Unit	Topics	Contact Hours	CLOs
I	Python and Engineering, Modular Programming, Introduction to python, Installation, Python as a calculator, Modules **Data Types** Introduction to various data types, Logical, Numeric , Sequences , Set and Frozen Set, Mappings and Null object	15	CLO1
II	**Operators** Introduction, Concepts of Variables, Assignment, Arithmetic and Logical , Membership, Identity, Bitwise operators **Arrays** **I**ntroduction, Numpy, adarray, automatic creation of arrays, Numerical ranges, broadcasting, indexing , slicing, masking, copying, some basic operations	15	CLO2
III	**Plotting** Introduction, Matpltolib, basic plots, histograms, bar charts, pie charts, polar plots, subplots, saving a plot file, displaying on web servers, working in object mode, logarithmic plots, contour plots, 3d plots, other libraries	15	CLO3
IV	**Functions and Loops** Introduction, defining functions, multi-input multi-output functions,Local and global variables, concept of loops, file I?O	15	CLO4
	Total Contact Hours	60	

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. "Introduction to Python-for Scientists and Engineers" by Sandeep Nagar (2006), Independently Published
2. Course No. 6.189, MIT Opencourseware, A Gentle Introduction to Programming using Python, (A Gentle Introduction to Programming Using Python | Electrical Engineering and Computer Science | MIT OpenCourseWare)

Evaluation Method

Outcomes	**Internal Assessment (30 Marks)**			**End Semester Examination (70 Marks)**
	Mid Term Exam	Seminar/Presentation/ Assignment/Quiz/Test	**Class Participation**	**SEE**
Marks:	**15**	**10**	**5**	**70**
CLO1	5	2.5	-	17
CLO2	5	2.5	-	17
CLO3	2.5	2.5		18
CLO4	2.5	2.5		18

w.e.f. Session: 2025-26			
Part A - Introduction			
Name of Programme	M.Sc. Electronic Science		
Semester	Fourth		
Name of the Course	Advanced Materials for VLSI		
Course Code	M24-ELE-405		
Course Type	DEC-4		
Level of the course	500-599		
Pre-requisite for the course	Knowledge of IC Fabrication Technology		
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO 1: Describe the requirements of cleanrooms for IC fabrication CLO 2: Implement the Silicon wafer cleaning process for device fabrication CLO 3: Design and simulate the fabrication processes required for IC fabrication CLO 4: Explain process integration flow for different IC fabrication technologies		
Credits	Theory	Practical	Total
	4	0	4
Teaching Hours per week	4	0	4
Internal Assessment Marks	30	0	30
End Term Exam Marks	70	0	70
Max. Marks	100	0	100
Examination Time	3 hours		

Part B- Contents of the Course

Instructions for Paper- Setter: The examiner will set 9 questions asking two questions from each unit and one compulsory question by taking course learning outcomes (CLOs) into consideration. The compulsory question (Question No. 1) will consist at least 4 parts covering entire syllabus. The examinee will be required to attempt 5 questions, selecting one question from each unit and the compulsory question. All questions will carry equal marks.

Unit	Topics	Contact Hours	CLOs
I	Clean Room Technology, Clean Room Classifications, Design concepts, Clean Room Installations and Operations, Automation related facility systems, future trends.	15	CLO1
II	Wafer Cleaning Technology - Basic Concepts, Wet cleaning, Dry cleaning, Epitaxy, Fundamental Aspects, Conventional silicon epitaxy, low temperature, Epitaxy of silicon, selective epitaxial growth of Si, Characterization of epitaxial films.	15	CLO2
III	Process simulation, Introduction, Ion-implantation, Monte Carlo method, Diffusion and Oxidation, two-dimensional LOCOS simulation example, Epitaxy, Epitaxial doping model, Lithography, Optical projection lithography, Electron-beam lithography, Etching and deposition, future trends.	16	CLO3
IV	VLSI Process Integration, Fundamental considerations for IC Processing, building individual layer, integrating the process steps, miniaturizing VLSI circuits, NMOS IC technology, fabrication process sequence, special consideration for NMOS ICs, CMOS IC technology, Fabrication Process sequence, special considerations for CMOS ICs, MOS memory IC technology, dynamic memory, static memory, bipolar IC technology, fabrication process sequence, special considerations for bipolar ICs, Self-aligned bipolar structures, Integrated injection logic, IC fabrication, process monitoring future trends.	14	CLO4
	Total Contact Hours		60

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. VLSI Technology by S.M.Sze.
2. ULSI Technology by C.Y. Chang and S.M. Sze (McGraw Hill International)

Evaluation Method

Outcomes	**Internal Assessment (30 Marks)**			**End Semester Examination (70 Marks)**
	Mid Term Exam	Seminar/Presentation/ Assignment/Quiz/Test	**Class Participation**	**SEE**
Marks :	**15**	**10**	**5**	**70**
CLO1	5	-	-	15
CLO2	5	2.5	-	20
CLO3	5	2.5		20
CLO4		5		15

w.e.f. Session: 2025-26			
Part A - Introduction			
Name of Programme	M.Sc. Electronic Science		
Semester	Fourth		
Name of the Course	RF Microelectronics		
Course Code	M24-ELE-406		
Course Type	DEC-4		
Level of the course	500-599		
Pre-requisite for the course	NIL		
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO 1: Understand the concepts of RF microelectronic devices and components CLO 2: Develop essential design concepts of RF networks and microelectronic circuits CLO 3: Understand various techniques for RF noise theories and frequency conversion techniques CLO 4: Understand the concept of microwave Integrated circuits		
Credits	Theory	Practical	Total
	4	0	4
Teaching Hours per week	4	0	4
Internal Assessment Marks	30	0	30
End Term Exam Marks	70	0	70
Max. Marks	100	0	100
Examination Time	3 hours		

Part B- Contents of the Course

Instructions for Paper- Setter: The examiner will set 9 questions asking two questions from each unit and one compulsory question by taking course learning outcomes (CLOs) into consideration. The compulsory question (Question No. 1) will consist at least 4 parts covering entire syllabus. The examinee will be required to attempt 5 questions, selecting one question from each unit and the compulsory question. All questions will carry equal marks.

Unit	Topics	Contact Hours	CLOs
I	Importance of RF and wireless technology, IC design technology for RF circuits, RF Behavior of passive components, operation for passive components at RF Active RF Components, RF Diodes, RF BJTs, RF FET, HEMT Active RF component modelling, Transistor models,	15	CLO1
II	Circuit representation of two port RF / Microwave Networks, Low and high frequency parameters, Formulation and properties of s parameters, Shifting reference plans, Transmission matrix, Generalized scattering parameters, Passive Circuit design, Review of Smith chart Matching and Biasing networks, Impedence matching using discrete components, microstrip line matching networks, amplifier classes of operation, RF Transistor amplifier designs, Low Noise amplifiers, Stability consideration, Constant gain noise figure circles	15	CLO2
III	Noise considerations in active networks, Noise definition, noise sources. RF Microwave oscillator design, Oscillator versus amplifier design, Oscillation conditions, Design of transistor oscillators, Generator Tuning networks RF / Microwave Frequency conversion II : Mixer design, Mixer types, Conversion loss for SSB mixers, SSB mixer versus DSB mixers. One diode mixers, Two diode mixers, Four diode mixers, Eight diode mixers,	16	CLO3
	Frequency synthesizers, PLL, RF synthesizer architectures, Transceiver architectures, Receiver architectures, Transmitter architectures, RF /		

IV	Microwave IC design, Microwave ICs, MIC Materials, Types of MICs, Hybrid vs monolithic MICs, Case studies, Relating to design of different circuits employed in RF Microelectronics	14	CLO4
		Total Contact Hours	60

Part C-Learning Resources

Recommended Books/e-resources/LMS:

15. Behzad Razavi, "RF Microelectronics" Prentice Hall PTR , 1998
16. R.Ludwig, P.Bretchko, RF Circuit Design, Pearson Education Asia, 2000.
17. Matthew M. Radmanesh, Radio Frequency and Microwave Electronics Illustrated, Pearson Education (Asia) Ltd., 2001

Evaluation Method

Outcomes	**Internal Assessment (30 Marks)**			**End Semester Examination (70 Marks)**
	Mid Term Exam	Seminar/Presentation/ Assignment/Quiz/Test	**Class Participation**	**SEE**
Marks :	**15**	**10**	**5**	**70**
CLO1	5	-	-	15
CLO2	5	2.5	-	20
CLO3	5	2.5		20
CLO4		5		15

w.e.f. Session: 2025-26			
Part A - Introduction			
Name of Programme	M.Sc. Electronic Science		
Semester	Fourth		
Name of the Course	Nanoscience and Nanotechnology		
Course Code	M24-ELE-407		
Course Type	DEC-4		
Level of the course	500-599		
Pre-requisite for the course	NIL		
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO1 : Understand the basic concepts of Nanoscience and technology CLO2 : Uunderstand the synthesis of nanomaterials CLO3 : Characterize the nanomaterials CLO4 : explain the aapplications of Nanoscience and Nanotechnology		
Credits	Theory	Practical	Total
	4	0	4
Teaching Hours per week	4	0	4
Internal Assessment Marks	30	0	30
End Term Exam Marks	70	0	70
Max. Marks	100	0	100
Examination Time	3 hours		

Part B- Contents of the Course

Instructions for Paper- Setter: The examiner will set 9 questions asking two questions from each unit and one compulsory question by taking course learning outcomes (CLOs) into consideration. The compulsory question (Question No. 1) will consist at least 4 parts covering entire syllabus. The examinee will be required to attempt 5 questions, selecting one question from each unit and the compulsory question. All questions will carry equal marks.

Unit	Topics	Contact Hours	CLOs
I	Basic concepts of Nanoscience and technology: Historical development of nanomaterials, Molecular and crystalline structures- Bulk to surface transition and calculations, density of states, bandgap and dimensionality of nanomaterials, surface reconstruction, Properties and technological advantages of Nano materials, Nanostructures: Quantum wire, Quantum well, Quantum dot, Size Effects, Quantum confinement, Fraction of Surface Atoms, specific Surface Energy and Surface Stress, Effect on the Lattice Parameters.	15	CLO1
II	Processing of Nanomaterials: Chemical methods: Chemical reduction method, Colloids in solution, Langmuir-Blodgett (L-B) method, sol gel methods. Physical Methods: laser deposition. Physical Vapour deposition, hydrothermal/solvothermal methods, and Microwave Synthesis of materials. electrochemical methods.	15	CLO2
III	Characterization of Nanomaterials: Structural Characterization: Powder X-ray diffractometer, FTIR spectrometer – Raman Spectrometer - Stylus profilometer. Microscopic and	15	CLO3

	Surface Analysis Electron microscopes: scanning electron microscope (SEM), transmission electron microscope (TEM); Scanning Probe Microscopy: atomic force microscope (AFM), scanning tunnelling microscope (STM). Electrical Properties: Impedance Spectroscopy, Thermal and Optical Properties: Differential scanning calorimeter (DSC)- Thermogravimetric/Diffferential thermal analyzer (TG/DTA), UV-Visible spectrophotometer.		
IV	Applications of Nanoscience and Nanotechnology Energy conservation and storage, Nanoelectronic devices, semiconductor nanodevices, solar cells, environmental remediation through nanoparticles, Nanoporous polymers and their applications in water purification, Biomedical Nanotechnology, Nanotechnology in Agriculture - Precision farming, Nanofertilizers-Nanourea and mixed fertilizers, Nanopesticides, Nanoseed Science. Nanotechnology in Food industry – Nanopackaging for enhanced shelf life.	15	CLO4
Total Contact Hours		60	

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. The Chemistry of Nanomaterials: Synthesis, Properties and Applications, 2 Volume Set C. N. R. Rao (Editor), Achim Müller (Editor), Anthony K. Cheetham (Editor), 2004. Wiley Publisher.
2. Nanobiotechnology: Concepts, Applications and Perspectives, Christof M. Niemeyer (Editor), Chad A. Mirkin (Editor), Wiley Publishers, April 2004.
3. Nanotechnology: A Gentle Introduction to Next Big Idea, Mark Ratner and Daniel Ratner, Low Price edition, Third Impression, Pearson Education.
4. Zhong Lin Wang, Characterization of Nanophase Materials, Wiley-VCH, Verlag GmbH, Germany (2004).
5. Carl C. Koch, Nanostructured Materials: Processing, Properties and Potential Applications, Noyes Publications, William Andrew Publishing Norwich, New York, U.S.A (2002).
1. Hari Singh Nalwa, "Nanostructured Materials and Nanotechnology", Academic Press, 2002
2. Nanoparticles: From theory to applications – G. Schmidt, Wiley Weinheim , 2004

Evaluation Method

Outcomes	**Internal Assessment (30 Marks)**			**End Semester Examination (70 Marks)**
	Mid Term Exam	Seminar/Presentation/ Assignment/Quiz/Test	**Class Participation**	**SEE**
Marks :	**15**	**10**	**5**	**70**
CLO1	7.5	-	-	17
CLO2	7.5		-	17
CLO3		5		18
CLO4		5		18

w.e.f. Session: 2025-26			
Part A - Introduction			
Name of Programme	M.Sc. Electronic Science		
Semester	Fourth		
Name of the Course	Semiconductor Packaging: Technology & Materials		
Course Code	M24-ELE-408		
Course Type	DEC-4		
Level of the course	500-599		
Pre-requisite for the course	Knowledge of IC Fabrication Technology		
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO 1 : Understand various IC packaging types and technologies CLO 2 : Describe the packaging materials and interconnection types CLO 3 : Explain the thermal issues in the IC packages CLO 4: Compare the various packaging strategies		
Credits	Theory	Practical	Total
	4	0	4
Teaching Hours per week	4	0	4
Internal Assessment Marks	30	0	30
End Term Exam Marks	70	0	70
Max. Marks	100	0	100
Examination Time	3 hours		

Part B- Contents of the Course

Instructions for Paper- Setter: The examiner will set 9 questions asking two questions from each unit and one compulsory question by taking course learning outcomes (CLOs) into consideration. The compulsory question (Question No. 1) will consist at least 4 parts covering entire syllabus. The examinee will be required to attempt 5 questions, selecting one question from each unit and the compulsory question. All questions will carry equal marks.

Unit	Topics	Contact Hours	CLOs
I	**Introduction to IC Packaging Technologies:** Significance and role of packaging in electronics, Historical evolution of packaging technologies, **Packaging types:** Through-hole, Surface-Mount, Ball Grid Array (BGA)	15	CLO1
II	**Packaging Materials and Interconnection Techniques:** Materials used in semiconductor packaging, Wire bonding, flip-chip, and solder bump technologies	15	CLO2
III	**Thermal Management in IC Packaging:** Principles of thermal conduction and dissipation, Cooling methods and heat sink strategies,	16	CLO3
IV	**Packaging Types and Trade-offs:** Comparative analysis: Through-hole, SMT, and BGA, Mechanical, electrical, and thermal trade-offs	14	CLO4
	Total Contact Hours	60	

Part C-Learning Resources

Recommended Books/e-resources/LMS:

18. 1. John H. Lau. Semiconductor Advanced Packaging. Springer, 2021.
19. King-Ning Tu, Chih Chen, Hung-Ming Chen. Electronic Packaging Science and Technology. Wiley, 2022.

Evaluation Method

Outcomes	**Internal Assessment (30 Marks)**			**End Semester Examination (70 Marks)**
	Mid Term Exam	Seminar/Presentation/ Assignment/Quiz/Test	**Class Participation**	**SEE**
Marks :	**15**	**10**	**5**	**70**
CLO1	5	-	-	15
CLO2	5	2.5	-	20
CLO3	5	2.5		20
CLO4		5		15

w.e.f. session: 2025-26			
Part A - Introduction			
Name of Programme	M.Sc Electronic Science		
Semester	Fourth		
Name of the Course	Introduction to IOT		
Course Code	M24-ELE-409		
Course Type	DEC-5		
Level of the course	500-599		
Pre-requisite for the course (if any)	NONE		
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO 1: Ability to understand need and applications of the IOT CLO 2: Ability to Understand the various components of IOT CLO 3: Ability to understand various Technologies Associated with IOT CLO 4: Ability to Understand the IOT topologies		
Credits	Theory	Practical	Total
	4	0	4
Teaching Hours per week	4	0	4
Internal Assessment Marks	30	0	30
End Term Exam Marks	70	0	70
Max. Marks	100	0	100
Examination Time	3 hours		

Part B- Contents of the Course

Instructions for Paper- Setter: The examiner will set 9 questions asking two questions from each unit and one compulsory question by taking course learning outcomes (CLOs) into consideration. The compulsory question (Question No. 1) will consist at least 4 parts covering entire syllabus. The examinee will be required to attempt 5 questions, selecting one question from each unit and the compulsory question. All questions will carry equal marks.

Unit	Topics	Contact Hours	CLOs
I	**Unit I** **Basics of Networking** : Introduction, Network Types, Layered Network Models, Addressing, TCP/IP Transport layer **Basics of Network Security**: Introduction, Security, Network Confidentiality, Cryptography, Message Integrity and Authencity, Key Management, Internet Security, Firewall	15	CLO1
II	Brief about predecessor of IOT, Introduction and Evolution of IOT, Enabling IOT, IOT Networking Components, Addressing Strategies in IOT	15	CLO2
III	**IOT sensing and actuation:** Sensor and actuator characteristics, Sensor and Actuator Types **IOT Processing Topologies and Types :** Data format, Processing Toplologies, IOT Design and Selection Considerations, Processing Offloading, IOT connectivity and Communication Technologies	15	CLO3
IV	**Associate IOT Technologies** : Cloud Computing, Fog Computing Cloud Computing :Introduction, Virtualisation, Cloud Model, SLA , Cloud implementation Fog Computing : Introduction, Architecture, Fog Computing in IOT Case study of Agricultural, Vehicular and Healthcare IOT	15	CLO4
	Total Contact Hours	60	

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. S. Misra, A. Mukherjee, and A. Roy, 2020. *Introduction to IoT*. Cambridge University Press.
2. S. Misra, C. Roy, and A. Mukherjee, 2020. *Introduction to Industrial Internet of Things and Industry 4.0.* CRC Press.

Evaluation Method

Outcomes	**Internal Assessment (30 Marks)**			**End Semester Examination (70 Marks)**
	Mid Term Exam	Seminar/Presentation/ Assignment/Quiz/Test	**Class Participation**	**SEE**
Marks:	**15**	**10**	**5**	**70**
CLO1	5	2.5	-	17
CLO2	5	2.5	-	17
CLO3	2.5	2.5		18
CLO4	2.5	2.5		18

w.e.f. Session: 2025-26			
Part A – Introduction			
Name of Programme	M.Sc. Electronic Science		
Semester	Fourth		
Name of the Course	Optical Fiber Communication		
Course Code	M24-ELE-410		
Course Type	DEC-5		
Level of the course	500-599		
Pre-requisite for the course	NIL		
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CO1: Understand the basic communication systems, principals and applications of optical fibers. CO2: Explain the dispersion and attenuation in optical fibers CO3: Understand various laser and LED structures and their characteristics, efficiency and reliability CO4: Explain the modulation and demodulation of Optical fiber systems & future developments		
Credits	Theory	Practical	Total
	4	0	4
Teaching Hours per week	4	0	4
Internal Assessment Marks	30	0	30
End Term Exam Marks	70	0	70
Max. Marks	100	0	100
Examination Time	3 hours		

Part B- Contents of the Course

Instructions for Paper- Setter: The examiner will set 9 questions asking two questions from each unit and one compulsory question by taking course learning outcomes (CLOs) into consideration. The compulsory question (Question No. 1) will consist at least 4 parts covering entire syllabus. The examinee will be required to attempt 5 questions, selecting one question from each unit and the compulsory question. All questions will carry equal marks.

Unit	Topics	Contact Hours	CLOs
I	Optical communication, Introduction, the measurement of information & capacity of a telecommunication channel, communication system architecture, the basic communication system, Optical communication system, the economic merits, optical fibers digital telecommunication system, analogue system, application & future developments, optical satellite communication.	15	CLO1
II	Elementary discussion of propagation in Fibers, Propagation a ray model, signal degradation in optical fibers, Material dispersion, the combined effect of material dispersion & multipath dispersion, RMS pulse widths & frequency response, attenuation in optical fibers, attenuation mechanisms, assessment of silica fibers & cables, power launching and coupling, fiber connectors, splices & couples.	15	CLO2
III	Semiconductor lasers for optical communication, the development of stripe geometry lasers, direct modulation of Semiconductor lasers, optical & electrical characterization of stripe geometry, sources for longer	15	CLO3

	wavelength LED's efficiency of DHLED. LED structures, characteristics, reliability.		
IV	Optical fiber systems, intensity modulation/direct detection, the optical transmitter circuit, the optical receiver circuit, digital systems, planning consideration, analog system, coherent optical fiber system, detection principles, modulation formats, Demodulation schemes, receiver sensitivities, optical fiber communication application & future developments.	15	CLO4
Total Contact Hours		60	

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. Optical fiber communications (Principle and Practice) 2nd edition-John M.Senior (Prentice Hall India Pvt. Ltd, New Delhi).
2. Optical Communication Systems Second edition-John Gowar (Prentice Hall India Pvt. Ltd, New Delhi).
3. Optical Fiber Communications - Gerd Keiser (McGraw Hill International editions, Singapore).
4. Fundamental of optical fiber communication second edition-Michael K.Barnoski (Academic Press,Orlando).
5. Fiber Optic Communication Systems-Govind P.Agarwal (John Wiley & Sons, Singapore).

Evaluation Method

Outcomes	Internal Assessment (30 Marks)			End Semester Examination (70 Marks)
	Mid Term Exam	Seminar/Presentation/ Assignment/Quiz/Test	Class Participation	SEE
Marks :	15	10	5	70
CLO1	7.5	-	-	17
CLO2	7.5		-	17
CLO3		5		18
CLO4		5		18

w.e.f. Session: 2025-26			
Part A - Introduction			
Name of Programme	M.Sc. Electronic Science		
Semester	Fourth		
Name of the Course	Mobile and data communication		
Course Code	M24-ELE-411		
Course Type	DEC-5		
Level of the course	500-599		
Pre-requisite for the course	NIL		
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CO1: Understand the concepts of mobile telephone CO2: Understand cellular technologies like 4G, 5G etc. CO3: Explain the basics of Data Communications CO4: Understand network layer, transport layer and application layer of communication		
Credits	Theory	Practical	Total
	4	0	4
Teaching Hours per week	4	0	4
Internal Assessment Marks	30	0	30
End Term Exam Marks	70	0	70
Max. Marks	100	0	100
Examination Time	3 hours		

Part B- Contents of the Course

Instructions for Paper- Setter: The examiner will set 9 questions asking two questions from each unit and one compulsory question by taking course learning outcomes (CLOs) into consideration. The compulsory question (Question No. 1) will consist at least 4 parts covering entire syllabus. The examinee will be required to attempt 5 questions, selecting one question from each unit and the compulsory question. All questions will carry equal marks.

Unit	Topics	Contact Hours	CLOs
I	Introduction, Mobile telephone Service, Cellular Telephone, Frequency reuse, Interference, Cell splitting, Sectoring, Segmentation and Dualisation, Cellular System Topology, Roaming and Hands offs, Cellular telephone network components, Cellular telephone call processing, Digital Cellular Telephone, SMS, GSM, GPRS, CDMA and EDGE architecture.	15	CLO1
II	Telecommunication Network management overview, Wireless Network fundamentals, OSI model layers, architecture, broadband systems. Introduction to Emerging technologies IP multimedia systems, GSM/CDMA, Wi-Fi, Wi-Max, Blue Tooth, 3G/4G &5G Next Gen. Networks (NGN), IP/ mobile TV	15	CLO2
III	Data Communications: Components, standards and organizations, Network Classification, Network Topologies; network protocol; layered network architecture; overview of OSI reference model; overview of TCP/IP protocol suite. Physical Layer: Cabling, Network Interface Card, Transmission Media Devices-Repeater, Hub, Bridge, Switch, Router, Gateway.	15	CLO3
IV	Data Networking: Virtual Circuits and Datagram approach, IP addressing methods -Subnetting; Routing Algorithms (adaptive and non-adaptive); Network Layer	15	CLO4

	Protocols: IPV4 and IPV6. Transport Layer: Process to Process Delivery: UDP; TCP, congestion control and Quality of service. Application Layer: Client Server Model, Socket Interface, Domain Name System (DNS): Electronic Mail (SMTP), file transfer (FTP), HTTP and WWW.		
Total Contact Hours		60	

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. Mobile Cellular Telecommunication: Analog and Digital Systems by W.C.Y Lee, Mc Graw- Hill.
2. Mobile Communications by Jochen Schiller, Pearson Education.
3. Electronic Communications Systems by Wayne Tomasi, Pearson Education
4. Rappaport. T.S., "Wireless communications", Pearson Education, 2003.
5. Gordon L. Stuber, "Principles of Mobile Communication", Springer International Ltd., 2001.
6. Andrea Goldsmith, Wireless Communications, Cambridge University Press, 2007.
7. Future Developments in Telecommunication, J. Martin, Prentice Hall

Evaluation Method

Outcomes	**Internal Assessment (30 Marks)**			**End Semester Examination (70 Marks)**
	Mid Term Exam	Seminar/Presentation/ Assignment/Quiz/Test	**Class Participation**	**SEE**
Marks :	**15**	**10**	**5**	**70**
CLO1	7.5	-	-	17
CLO2	7.5		-	17
CLO3		5		18
CLO4		5		18

w.e.f. Session: 2025-26			
Part A - Introduction			
Name of Programme	M.Sc. Electronic Science		
Semester	Fourth		
Name of the Course	Verification Tools & Technologies		
Course Code	M24-ELE-412		
Course Type	DEC-5		
Level of the course	500-599		
Pre-requisite for the course	NIL		
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CLO 1 : understand the importance of verification in digital design CLO 2 : learn simulation tools for basic verification of digital systems CLO 3 : explain the formal verification processes CLO 4: use industry standard verification tools for digital verification		
Credits	Theory	Practical	Total
	4	0	4
Teaching Hours per week	4	0	4
Internal Assessment Marks	30	0	30
End Term Exam Marks	70	0	70
Max. Marks	100	0	100
Examination Time	3 hours		

Part B- Contents of the Course

Instructions for Paper- Setter: The examiner will set 9 questions asking two questions from each unit and one compulsory question by taking course learning outcomes (CLOs) into consideration. The compulsory question (Question No. 1) will consist at least 4 parts covering entire syllabus. The examinee will be required to attempt 5 questions, selecting one question from each unit and the compulsory question. All questions will carry equal marks.

Unit	Topics	Contact Hours	CLOs
I	**Introduction to Verification in Digital Design:** Importance of verification in the design lifecycle, Functional verification concepts and terminology, Overview of simulation-based verification	15	CLO1
II	**Simulation Tools and Basic Verification Techniques:** Hands-on with tools like ModelSim and VCS, Writing testbenches, generating stimulus, analyzing output	15	CLO2
III	**Formal Verification Principles:** Concepts of formal verification, model checking, and theorem proving, Comparison of formal vs. simulation methods, formal verification on small hardware designs	16	CLO3
IV	**Industry-Standard Verification Tools:** Overview and comparison of tools like Questa, VCS, JasperGold Functionalities such as coverage analysis, waveforms, and debugging	14	CLO4
	Total Contact Hours	60	

Part C-Learning Resources

Recommended Books/e-resources/LMS:

20. Douglas Perry. Applied Formal Verification. McGraw Hill, 2005.
21. Graham Birtwistle. VLSI Specification, Verification and Synthesis. Springer, 2012.
22. Thomas Kropf. Introduction to Formal Hardware Verification. Springer, 2013.
23. Erik Seligman. Formal Verification. Elsevier, 2023.

Evaluation Method

Outcomes	**Internal Assessment (30 Marks)**			**End Semester Examination (70 Marks)**
	Mid Term Exam	Seminar/Presentation/ Assignment/Quiz/Test	**Class Participation**	**SEE**
Marks :	**15**	**10**	**5**	**70**
CLO1	5	-	-	15
CLO2	5	2.5	-	20
CLO3	5	2.5		20
CLO4		5		15

w.e.f. Session: 2025-26			
Part A – Introduction			
Name of Programme	M.Sc. Electronic Science		
Semester	Fourth		
Name of the Course	Research Ethics		
Course Code	M24-ELE-413		
Course Type	EEC		
Level of the course	500-599		
Pre-requisite for the course	NIL		
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CO1: Understand the research ethics. CO2: Understand the scientific conduct in research. CO3: Familiarize with Intellectual honesty and research integrity CO4: Become aware about the publication Misconduct.		
Credits	Theory	Practical	Total
	2	0	2
Teaching Hours per week	2	0	2
Internal Assessment Marks	15	0	15
End Term Exam Marks	35	0	35
Max. Marks	50	0	50
Examination Time	3 hours		

Part B- Contents of the Course

Instructions for Paper- Setter: The examiner will set 8 questions asking four questions from each unit by taking course learning outcomes (CLOs) into consideration. The examinee will be required to attempt 5 questions in all, selecting at least two questions from each unit. All questions will carry equal marks.

Unit	Topics	Contact Hours	CLOs
I	Ethics: definition, moral philosophy, nature of moral judgements and reactions, Research Ethics: Informed consent; Confidentiality and privacy. Record-Keeping. Ethics with respect to science and research	6	CLO1 CLO2
II	Intellectual honesty and research integrity: Intellectual Property Rights (IPR): Copyright, patents, trademarks; Ethical considerations in intellectual property; Salient features of Indian and international laws of IPR. Scientific Misconduct: Fabrication, falsification, plagiarism. misrepresentation; Duplicate publication, conflict of interest: Research mismanagement, biased reporting, Peer review manipulation, data theft, and misuse.	6	CLO3 CLO4
	Total Contact Hours	12	

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. Bird, A. (2006). Philosophy of Science. Routledge.
2. Chaddah, P. (2018) Ethics in Competitive Research: Do not get scooped; do not get plagiarised.
3. Deakin, L. (2014). Best practice guidelines on publishing ethics: A publisher's perspective.

Wiley.
4. Indian National Science Academy. 2019. Ethics in Science Education, Research and Governance.
2. Research ethics for social scientists: Between ethical conduct and regulatory compliance. Sage.
3. MacIntyre, A. (198). A short history of ethics. Routledge.

Evaluation Method

Outcomes	**Internal Assessment (15 Marks)**			**End Semester Examination (35 Marks)**
	Mid Term Exam	Seminar/Presentation/ Assignment/Quiz/Test	**Class Participation**	**SEE**
Marks :	**6**	**6**	**3**	**35**
CLO1	3	-	-	9
CLO2	3		-	9
CLO3		3		8
CLO4		3		9

Session: 2024-25			
Part A - Introduction			
Name of Programme	M.Sc. Electronic Science		
Semester	Fourth		
Name of the Course	Dissertation		
Course Code	M24-ELE-414		
Course Type	Dissertation/Project Work		
Level of the course	500-599		
Pre-requisite for the course			
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CO1: Ability to engage in independent study to research literature in the identified domain. CO2: Ability to identify the community that shall benefit through the solution to the identified engineering problem and demonstrate concern for environment. CO3: Ability to engage in independent study to identify the mathematical concepts, science concepts, engineering concepts and management principles necessary to solve the identified engineering problem CO4: Ability to analyze and interpret results of experiments conducted on the designed solution(s) to arrive at valid conclusions CO5: Ability to perform the budget analysis of the project through the utilization of resources (finance, power, area, bandwidth, weight, size, any other) CO6: Ability to engage in effective written communication through the project report, journal/poster presentation of the project work CO7: Ability to engage in effective oral communication through presentation and demonstration of the project work CO8: Ability to perform in the team, contribute to the team and mentor/lead the team CO9: Ability to abide by the norms of professional ethics		
Credits	Theory	Practical	Total
			12
Teaching Hours per week			
Evaluation of Dissertation & End Term Exam Marks (Viva Voce)			300
Max. Marks			300
Examination Time	3 hours		

Part B- Contents of the Course

The student will undertake independent research on a chosen topic under faculty / Mentor supervision at and Industry/University or an R7D organization. The student will write a well structured dissertation that would reflect critical thinking, analytical depth, and scholarly engagement with primary and secondary text.

w.e.f. Session: 2025-26			
Part A – Introduction			
Name of Programme	M.Sc. Electronic Science		
Semester	Third		
Name of the Course	Fundamentals of Nanomaterials		
Course Code	M24-OEC-313		
Course Type	OEC		
Level of the course	500-599		
Pre-requisite for the course	NIL		
Course Learning Outcomes (CLO) After completing this course, the learner will be able to:	CO1: Explain general concepts of Nanomaterials CO2: Synthesize nanomaterials CO3: Identify the phase using search peak analysis from XRD pattern CO4: Interpret the characterized results		
Credits	Theory	Practical	Total
	2	0	2
Teaching Hours per week	2	0	2
Internal Assessment Marks	15	0	15
End Term Exam Marks	35	0	35
Max. Marks	50	0	50
Examination Time	3 hours		

Part B- Contents of the Course

Instructions for Paper- Setter: The examiner will set 8 questions asking four questions from each unit by taking course learning outcomes (CLOs) into consideration. The examinee will be required to attempt 5 questions in all, selecting at least two questions from each unit. All questions will carry equal marks.

Unit	Topics	Contact Hours	CLOs
I	Basic concepts of Nano science and technology, Properties and technological advantages of Nano materials, Nanostructures: Quantum wire, Quantum well, Quantum dot, Size Effects, Quantum confinement, Fraction of Surface Atoms, specific Surface Energy and Surface Stress, Material processing by Sol – Gel method, Chemical Vapour deposition and Physical Vapour deposition, hydrothermal/solvothermal methods.	6	CLO1 CLO2
II	Experimental approaches and data interpretation: X ray characterization, Scanning probe microscope (AFM and STM), Electron microscopy: SEM/TEM, high resolution imaging, Differential scanning calorimeter (DSC) Thermogravimetric/Differential thermal analyzer (TG/DTA), UV-Visible spectrophotometer, FTIR	6	CLO3 CLO4
Total Contact Hours		12	

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1 C. N. R. Rao, A. Mu¨ller, A. K. Cheetham, The Chemistry of Nanomaterials: Synthesis, Properties and Applications, Volume 1, Wiley-VCH, Verlag GmbH, Germany (2004).

2 C. Bre´chignac P. Houdy M. Lahmani, Nanomaterials and Nanochemistry, Springer Berlin Heidelberg, Germany (2006).
3 Guozhong Cao, Nanostructures & Nanomaterials Synthesis, Properties G;Z: Applications, World Scientific Publishing Private, Ltd., Singapore (2004).
4 Zhong Lin Wang, Characterization Of Nanophase Materials, Wiley-VCH, Verlag GmbH, Germany (2004). 5) Carl C. Koch, Nanostructured Materials: Processing, Properties and Potential Applications, Noyes Publications, William Andrew Publishing Norwich, New York, U.S.A (2002).
5. Hari Singh Nalwa, "Nanostructured Materials and Nanotechnology", Academic Press, 2002

Evaluation Method

Outcomes	**Internal Assessment (15 Marks)**			**End Semester Examination (35 Marks)**
	Mid Term Exam	Seminar/Presentation/ Assignment/Quiz/Test	**Class Participation**	**SEE**
Marks :	**6**	**6**	**3**	**35**
CLO1	3	-	-	9
CLO2	3		-	9
CLO3		3		8
CLO4		3		9